Electrical Characterization of Ge-FinFET Transistor Based on Nanoscale Channel Dimensions

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Nano-electronic applications have benefited enormously from the great advancement in the emerging Nano-technology industry. The tremendous downsizing of the transistors’ dimensions has enabled the placement of over 100 million transistors on a single chip thus reduced cost, increased functionality and enhanced performance of integrated circuits (ICs). However, reducing size of the conventional planar transistors would be exceptionally challenging due to leakages electrostatics and other fabrication issues. Fin Field Effect Transistor (FinFET) shows a great potential in scalability and manufacturability as a promising candidate and a successor to conventional planar devices in nanoscale technologies. The structure of FinFET provides superior electrical control over the channel conduction, thus it has attracted widespread interest of researchers in both academia and industry. However, aggressively scaling down of channel dimensions, will degrade the overall performance due to detrimental short channel effects. In this paper, we investigate the impact of downsizing of nano-channel dimensions of Germanium Fin Feld Effect Transistor (Ge-FinFET) on electrical characteristics of the transistor, namely, $I_{on}/I_{off}$ ratio, Subthreshold Swing (SS), Threshold voltage ($V_{T}$), and Drain-induced barrier lowering (DIBL). MuGFET simulation tool was utilized to conduct a simulation study to achieve optimal channel dimensions by considering channel length ($L$), width ($W$), and oxide thickness ($t_{ox}$) individually. In addition, the effects of simultaneous consideration of all dimensions by exploiting a scaling factor, $K$ was evaluated. According to the obtained simulation results, the best performance of Ge-FinFET was achieved at a minimal scaling factor, $K = 0.25$ with 5 nm channel length, 2.5 nm width, and 0.625 nm oxide thickness.

**Keywords:** Ge- FinFET, Channel dimensions, $I_{on}/I_{off}$ ratio, Subthreshold swing, MuGFET.

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1. **INTRODUCTION**

Fin Field Effect Transistor (FinFET) has shown a great potential in scalability and manufacturability as a promising candidate in nanoscale complementary metal-oxide-semiconductor (CMOS) technologies [1, 2]. The structure of FinFET provides superior electrical control over the channel conduction, thus, it has attracted widespread interest from researchers in both academia and industry [3]. However, tremendous downsizing of channel dimensions, mainly the channel length, will degrade the overall performance due to detrimental short channel effects (SCEs) such as to leakages, energy consumption, electrostatics, in addition to other fabrication issues [4-6].

The applications of Nano-electronic have benefited enormously from the great advancement in the emerging Nano-technology industry [7, 8]. The name of FinFET technology comes from the fact that the structure of FET looks like a set of fins when viewed [9]. Such type of gate structure provides an improved electrical control over the channel conduction and it helps in reducing leakage current levels and overcoming some other issues related to short-channel such as electrostatic limits and source-to-drain tunneling [10]. These issues represent constraints in the design and fabrication of transistors beyond Nano-Dimensional channel length in conventional MOSFET [11, 12].

More new FET structures are being explored on a large scale. One of these structures was the FinFET, which has attracted a widespread of researchers in both academia and industry of semiconductors [13], thanks to the vertical fin that determines the source channel discharge. It will be appreciated that the FinFETs can be used with (25 nm) gate length as they have the ability to provide high current immunity and high immunity to SCEs [6]. FinFET was born as a result of the continuous increase in integration levels. Control over the reduced channel length of FinFET is more complicated and more important. This is because the conduction occurs in two parallel channels that are in vertical planes the conduction remaining parallel to the substrate surface between drain and source area. The drain current is flowing on both sides of the fin is a way to increase the discharge source for the same area in the channel region. Thus, efforts and attentions to finding a solution for this issues are highly increased.

In this paper, we simulate and analyze the effects of reducing channel dimensions [length ($L$), width ($W$), and oxide thickness ($t_{ox}$)] of Germanium Fin Feld Effect Transistor (Ge-FinFET) on its performance in terms of FOUR (4) electrical characteristics, namely, (i) $I_{on}/I_{off}$ ratio, (ii) Subthreshold Swing (SS), (iii) Threshold voltage ($V_{T}$), and (iv) Drain-induced barrier lowering (DIBL). Moreover, we propose a scaling factor $K$ to downscale all dimensions ($L$, $W$, and $t_{ox}$) as once and detect the best performance based on the selected scaling factor. According to simulation results, we have designed the best nanoscale channel dimensions of Ge-FinFET based on the highest $I_{on}/I_{off}$ ratio and the best SS characteristics.
The simulation
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channel concentration
Channel length
Table
were
oxide thickness wa
varying
ulation scenarios
The setting
the temperature of 300
of variable channel dimensions, namely; channel
length, width and oxide thickness in addition to scaling
factor of the Ge-FinFET transistor, are determined. In
particular, the \( I_d-V_d \) characteristics of Ge-FinFET at
the temperature of 300 K are simulated and analyzed.
The setting of simulation parameters in this study are
listed in Table 1.
In order to evaluate electrical characteristics of Ge-
FinFET based on channel’s dimensions, FOUR (4) sim-
ulation scenarios were designed for different simulation
parameters. The first scenario focused on impact of
varying channel length only, while keeping other di-
ensions (\( W \) and \( T_{ox} \)) constant. The second scenario
investigated electrical characteristics based on various
channel widths, while both length and oxide thickness
of channel were unchanged. In the third scenario, only
oxide thickness was changed and other dimensions
were kept constant. The last scenario was designed for
simultaneous consideration of all dimensions, \( L, W, \) and \( T_\text{ox} \) by changing scaling factor \( K \) to decrease all
dimensions and evaluate transistor performance for
each value of \( K \).
Table 1 – Simulation parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length, ( L )</td>
<td>(10, 15, 20 and 40) nm</td>
</tr>
<tr>
<td>Channel width, ( W )</td>
<td>(5, 10, 12, and 20) nm</td>
</tr>
<tr>
<td>Oxide thickness, ( T_{ox} )</td>
<td>(1.5, 2.5, 5 and 7) nm</td>
</tr>
<tr>
<td>Scaling factor, ( K )</td>
<td>(0.25, 0.5, 0.75 and 1.00)</td>
</tr>
<tr>
<td>channel concentration ( p )-type</td>
<td>( 10^{16} ) cm(^{-3} )</td>
</tr>
<tr>
<td>channel concentration ( n )-type</td>
<td>( 10^{19} ) cm(^{-3} )</td>
</tr>
</tbody>
</table>

3. RESULTS AND DISCUSSION

3.1 Downscaling Channel Length Scenario

In this scenario, the impact of scaling down of chan-
nel length \( L \) on the characteristics of Ge FinFET has
been studied. The channel length \( L \) was changed be-
tween 10 and 40 nm, whereas \( W \) and \( T_{ox} \) were kept
constant at default values of MuGFET which are 5 nm
and 2.5 nm, respectively. The simulation of transfer
characteristics (drain current \( I_d \) – gate voltage \( V_g \))
has been conducted with different channel lengths \( L \).
Based on the obtained results, the \( I_{on}/I_{off} \) ratio pro-
portionally increases with channel length at both voltages,
\( V_{dd} = 5 \) V and 0.5 V. As illustrated in Table 2, the
maximum value of the \( I_{on}/I_{off} \) ratio is more than \( 10^4 \)
at \( L = 40 \) nm. For \( L \) range from 10 to 30 nm, the highest
\( I_{on}/I_{off} \) ratio is for \( V_{dd} = 0.5 \) V, while for 30 to 40 nm \( L \)
range the highest \( I_{on}/I_{off} \) ratio occurs for \( V_{dd} = 5 \) V.
The relation between SS characteristic and channel lengths
is also investigated. Results show that the SS is
improved as the channel length increased and reached to
65 mV/dec the nearest value to the ideal SS at
\( L = 40 \) nm. Similarly, the threshold voltage (\( V_T \)) gains
some increment with increasing the channel length,
where \( V_T = 0.43 \) V at the maximum \( L \) of 40 nm and
\( V_T = 0.20 \) V at the minimum \( L \) of 10 nm. Conversely,
induced-drain lowering (DIBL) of the Ge-FinFET
reduces with increasing channel length and reaches to
4.8 mV/N at \( L = 40 \) nm.

Table 2 – Summary of main findings

<table>
<thead>
<tr>
<th>Scenario</th>
<th>Characteristics</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scenario 1</td>
<td>( I_{on}/I_{off} )</td>
<td>2.29( \times )10(^4 )</td>
</tr>
<tr>
<td>( L )</td>
<td>SS, mV/dec</td>
<td>65</td>
</tr>
<tr>
<td>Best ( L ), nm</td>
<td></td>
<td>40</td>
</tr>
<tr>
<td>Scenario 2</td>
<td>( I_{on}/I_{off} )</td>
<td>2.29( \times )10(^3 )</td>
</tr>
<tr>
<td>( W )</td>
<td>SS, mV/dec</td>
<td>62</td>
</tr>
<tr>
<td>Best ( W ), nm</td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>Scenario 3</td>
<td>( I_{on}/I_{off} )</td>
<td>3.53( \times )10(^3 )</td>
</tr>
<tr>
<td>( T_{ox} )</td>
<td>SS, mV/dec</td>
<td>67</td>
</tr>
<tr>
<td>Best ( T_{ox} ), nm</td>
<td></td>
<td>1.5</td>
</tr>
<tr>
<td>Scenario 4</td>
<td>( I_{on}/I_{off} )</td>
<td>3.56( \times )10(^4 )</td>
</tr>
<tr>
<td>( K )</td>
<td>SS, mV/dec</td>
<td>68.9</td>
</tr>
<tr>
<td>Best ( K )</td>
<td></td>
<td>0.25</td>
</tr>
</tbody>
</table>

According to the obtained characteristics in this
scenario, the best performance in terms of all perfor-
ance metrics can be achieved in case with 40 nm
channel length. Therefore, it is obvious that with consid-
ering channel length only, we cannot go far in downsca-
ling channel dimensions due to the degradation of tran-
sistor performance, especially in short length channel.

3.2 Downscaling Channel Width Scenario

The impact of scaling down channel width \( W \) on the considered performance metrics of Ge-FinFET has been
evaluated in this scenario. The value of \( W \) was de-
creased from 20 nm to 5 nm, while \( L \) and \( T_{ox} \) were
fixed to 40 nm and 2.5 nm, respectively. Unlike the previous scenario, the downscaling of channel width
improved the performance of transistor in terms of all
characteristics. The best performance was achieved
with the smallest channel width, \( W = 5 \) nm where the \( I_{ON}/I_{OFF} \) ratio is more than \( 10^2 \) and SS = 62 mV/dec according to the results in Table 3.

The improvement in Ge-FinFET with shrinking channel width is also obvious in terms of threshold voltage and DIBL. The \( V_T \) is inversely proportional to channel width, where \( V_T = 0.435 \) V at the minimum channel width of 5 nm and \( V_T = 0.24 \) V at the maximum channel width of 20 nm. Meanwhile, the DIBL is proportional to channel width and it attains the minimum and best value of 4.9 mV/V/m when \( W = 20 \) nm.

### 3.3 Downsizing Channel Oxide Thickness Scenario

The behaviour of Ge-FinFET in terms of most electrical characteristics with scaling down channel oxide thickness is consistent with previous scenario of channel width variation. As the oxide thickness of channel decreased, characteristics were enhanced, even though the improvement is less comparing with the width-based scenario. For the simulation scenario carried out in this phase, the channel oxide thickness \( T_{OX} \) has been changed (1.5, 2.5, 5 and 7 nm), while both channel length and width were kept constant at 40 and 10 nm, respectively. The obtained results prove the variation of \( I_{ON}/I_{OFF} \) ratio with the channel oxide thickness. The best \( I_{ON}/I_{OFF} \) ratio was greater than \( 10^4 \) and was obtained with \( V_{DD} = 5 \) V at minimum \( T_{OX} = 1.5 \) nm and then decreased to \( 10^2 \) at \( T_{OX} = 7 \) nm. Almost similar results were obtained for 0.5 V voltage which represents the nearest voltage to OFF static voltage (0 V). We noticed from the results that for a channel oxide thickness \( T_{OX} = 1.5 \) nm the Ge-FinFET has shown better SS characteristics with the best SS value of 67 mV/dec compared to other \( T_{OX} \) values. Conversely, the farthest value from ideal SS (69.5 mV/dec) occurred at \( T_{OX} = 7 \) nm, where SS is 229 mV/dec.

Furthermore, an improvement in terms of both \( V_T \) and DIBL characteristics of Ge-FinFET was achieved by decreasing channel oxide thickness. While the voltage threshold increased linearly with decreasing \( T_{OX} \), the DIBL was not consistent and its value fluctuating with different oxide thickness. The best and highest threshold voltage was \( V_T = 0.35 \) V at the smallest channel oxide thickness of 1.5 nm. Similarly, DIBL achieved the smallest value of 19 mV/V at the minimal \( T_{OX} \).

### 3.4 Scaling Factor of Channel Dimensions

According to the aforementioned scenarios, the best performance in terms of the considered electrical characteristics was achieved at channel length \( L = 40 \) nm, channel width \( W = 5 \) nm, and channel oxide thickness \( T_{OX} = 1.5 \) nm. Thus, Ge-FinFET has not achieved a proper performance with a shrinking channel length where it attains better performance at the longest channel case. In order to scaling down all channel dimensions as once, we have applied a scaling factor \( K \) on all dimensions including length, width and thickness. Following we study the electrical characteristics based on scaling factor, the reference value of \( K \) is defined as “1” with its highest channel dimensions. Then, all dimensions are scaling down to reach to new physical limits for the channel of Ge-FinFET. All corresponding dimensions to the defend scaling factors are shown in Table 3.

<table>
<thead>
<tr>
<th>( K )</th>
<th>( L, ) nm</th>
<th>( W, ) nm</th>
<th>( T_{OX}, ) nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>40</td>
<td>20</td>
<td>6</td>
</tr>
<tr>
<td>0.75</td>
<td>20</td>
<td>10</td>
<td>3</td>
</tr>
<tr>
<td>0.5</td>
<td>10</td>
<td>5</td>
<td>1.5</td>
</tr>
<tr>
<td>0.25</td>
<td>5</td>
<td>2.5</td>
<td>0.625</td>
</tr>
</tbody>
</table>

![Fig. 1 – Impact of varying dimensions scaling factor of Ge-FinFET on \( I_{ON}/I_{OFF} \) ratio](image1)

![Fig. 2 – Impact of varying dimensions scaling factor of Ge-FinFET on subthreshold swing](image2)

![Fig. 3 – Impact of varying dimensions scaling factor of Ge-FinFET on threshold voltage](image3)

Fig. 1 shows the relation between \( I_{ON}/I_{OFF} \) ratio with the scaling factor \( K \) from 0.25 to 1. Obviously, we can notice the improvement in \( I_{ON}/I_{OFF} \) characteristics with downsizing all channel dimensions together. The best value of \( I_{ON}/I_{OFF} \) ratio is higher than \( 10^4 \) which is achieved at scaling factor of \( K = 0.25 \) for both \( V_{DD} = 5 \) V and for \( V_{DD} = 0.5 \) V. The worst \( I_{ON}/I_{OFF} \) ratios, less than
were occurred at the reference value of scaling factor for both VDD voltages.

Fig. 4 – Impact of varying dimensions scaling factor of Ge-FinFET on drain-induced barrier lowering

Fig. 2 shows the worst SS characteristic value (100 mV/dec) that is obtained at $K = 1$. In contrast, the nearest value to the ideal SS is 68.9 mV/dec was acquired at $K = 0.25$. It can be notice that with increasing $K$, the SS value increases significantly. Likewise, the impact of changing Scaling Factor ($K$) on $V_T$ and DIBL is illustrated in Fig. 3, where the highest value of $V_T = 0.64$ V is obtained at $K = 0.25$, compared to the lowest value $V_T = 0.33$ V at $K = 1$. On the other hand, the DIBL value ranges from 356 mV/V to 111 mV/V between minimum and maximum value of $K$, respectively, with inconsistent behaviour in between as illustrated in Fig. 4.

REFERENCES


4. CONCLUSIONS

We have demonstrated the electrical characteristics of Ge-FinFET based on various channel dimensions. Our calculation of the best performance was achieved at highest $I_{ON/OFF}$ ratio and the nearest SS to the ideal value in different simulation scenarios using MoGFET. We have changed dimensions individually to study the impact of each ($L$, $W$, $T_{OX}$) on the different extracted characteristics ($I_{ON/OFF}$ ratio at two voltages, SS, $V_T$, and DIBL) of Ge-FinFET. In the following we have investigated the effect of scaling factor $K$ to scaling down all dimensions to their mammal value with appropriate performance. We observed that by variation of the dimensions scaling factor, it can be possible to design new physical limits for channel dimensions with increasing the $I_{ON/OFF}$ ratio and enhancing SS, $V_T$ and DIBL characteristics.

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відністю каналів, і, таким чином, привертає широкий інтерес дослідників як з наукової, так і з прикладної точки зору. Однак різке зменшення розмірів каналів призводить до погіршення загальної продуктивності за рахунок шкідливих ефектів короткого каналу. У даній роботі досліджено вплив зменшення розмірів каналів транзистора з германію (Ge-FinFET) на електричні характеристики транзистора, а саме на відношення $I_{ON}/I_{OFF}$, підпорогове коливання, порогову напругу та індуковане стоком зниження бар'єру. MuGFET був використаний у моделюванні для досягнення оптимальних розмірів каналу, враховуючи індивідуальну довжину каналу, ширину і товщину оксиду. Крім того, були оцінені ефекти одночасного розгляду усіх вимірів, використовуючи коефіцієнт масштабування. Згідно з отриманими результатами моделювання, найкраща продуктивність Ge-FinFET була досягена за мінімального коефіцієнта масштабування $K = 0.25$ з довжиною каналу 5 нм, шириною 2.5 нм і товщиною оксиду 0.625 нм.

Ключові слова: Ge-FinFET, Розміри каналів, $I_{ON}/I_{OFF}$ відношення, Підпорогове коливання, MuGFET.