

## Investigation and Design of Novel Comparator in Quantum-dot Cellular Automata Technology

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Quantum-dot cellular automata (QCA) technology is one of attractive emerging technologies that are suitable for low-power, and ultra-dense digital circuit's development. QCA Comparator plays an important role in the digital circuits. In this study, a new QCA comparator architecture is presented. This new architecture is carefully designed using three 3-input majority gates. The proposed QCA comparator architecture is simulated by using the QCADesigner tool version 2.0.3. The designed QCA comparator has 29 cells and the occupied area by circuit is  $0.04 \mu\text{m}^2$ . The results demonstrate that the developed QCA comparator architecture provides an improvement compared to other QCA comparator architectures in terms of the number of required cells.

**Keywords:** Nanotechnology, Quantum-dot cellular automata, Comparator, QCADesigner, Combinational logic.

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### 1. INTRODUCTION

Recently, the circuit design based on Quantum-dot Cellular Automata (QCA) has received a great deal of attention. So, several attempts have been directed towards design of arithmetic circuits such as adder [1-3], and comparators [4-6].

Comparators are extensively utilized circuit in the microcontrollers and Central Processing Units (CPUs) [7]. There are several attempts to improve the performance of the QCA comparator such as [4-6, 8-10].

The designed comparator in [5] is 1-bit comparator with 100 cells. Another designed comparator, which has been presented in [6], has two-layer structure with 79 cells. In [8], a 1-bit comparator has been designed with 73 cells. The designed comparator in [9] is composed of two 5-input majority gates and a 3-input majority gate with 43 cells. In [10], a 1-bit comparator with 81 cells is designed. However, these QCA comparator architectures have advantages, the performance of the QCA comparator can be improved as described in this paper.

This paper deals with QCA based comparator design. In this study, we design a new full QCA comparator. The developed QCA comparator is simulated using the QCADesigner tool version 2.0.3. The simulation results show that the proposed QCA comparator architecture has advantages in comparison with other QCA comparator architectures in terms of the number of required cells and occupied area.

The remaining of this paper is organized as follows: in section 2, the backgrounds of the proposed QCA circuit including QCA cells, QCA clock, QCA gate, and QCA comparator is presented. Moreover, this section investigates the previous QCA comparator architectures. In section 3, the proposed QCA comparator is presented. In section 4, the simulation results are presented and compared with other works. Finally, section 5 concludes this paper.

### 2. BACKGROUND

#### 2.1 The QCA Cells

The basic element in the QCA technology is a cell. The cells in the QCA technology are formed with 4 quantum dots. Each dot in the QCA cell represents a position where an electron can be positioned [11, 12]. In this technology, each cell is charged with two free electrons. Electrons can tunnel between quantum dots [6]. It should be noted that there are two possible steady states for each cell. Fig. 1 shows a QCA cell and these two possible steady states.

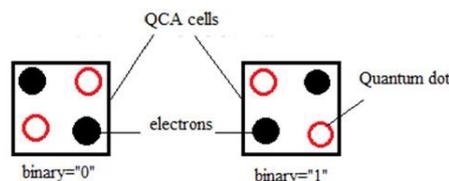


Fig. 1 – The possible polarizations for the QCA cell [2, 6]

The polarization of the QCA cell, which is shown by  $P$ , can be computed based on the distribution probability of the electron locations. Note that,  $P = -1$  and  $P = 1$  represent the binary value 0 and 1, respectively [2, 6, 13].

Equation (1) shows the calculation method for the polarization in the QCA cell [6, 13].

$$P = \frac{(p_1 + p_3) - (p_2 + p_4)}{p_1 + p_2 + p_3 + p_4} \quad (1)$$

Here  $p_i$  denotes the  $i$ th quantum-dot charge ( $p_i = 1$  to show presentation of electron, otherwise it is 0).

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2.2 QCA Clock

In the QCA technology, clock is utilized for information flow controlling [14]. The QCA clock is divided into four phases. Fig. 2 shows the clock zones in the QCA technology [14].

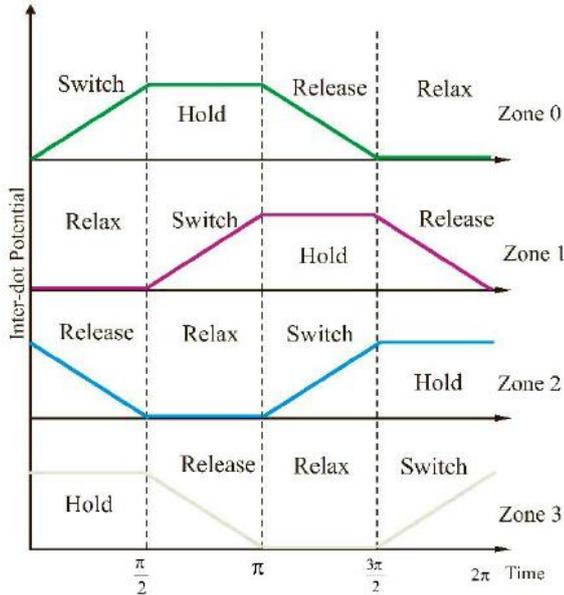


Fig. 2 – The clock zones in the QCA technology [14]

As it is shown in Fig. 2, the cells are begin depolarized during the Switch phase. In this phase, the potential barriers within cells are low. In the Hold phase, the electrons cannot change their positions within the cell. However, they can influence other cells. Note that, the barrier potential is gradually become lower at the end of this phase. So, during the Release phase, the cells begin to depolarize. The clock phase changes to the Relax phase, when the barriers are in their lowest level. So, the cells are remain in this state and the cell barriers are remain at their lowest level [2, 14].

2.3 The QCA Gates

The majority gate is a basic QCA logic gate. Figure 3 shows the 3-input QCA majority gate [15].

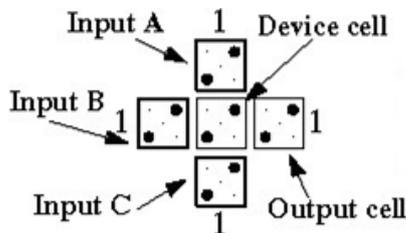


Fig. 3 – The 3-input QCA majority gate [15]

The majority gate is a logical gate utilized in the complex circuits. The output of the majority gate is true if and only if more than 50% of its inputs are true [15]. The basic majority gate takes input as 3, 5, 7... (2n + 1) bits. The functionality of the 3-input majority gate is defined as follows [15]:

$$\text{Maj}(A, B, C) = AB + AC + BC \quad (2)$$

Other types of gates, namely AND gate and OR gate, are constructed by using the majority gate with fixed polarization on one of its inputs. On the other hand, a NOT gate is fundamentally different from the majority gate. Figure 4 shows these gates [2].

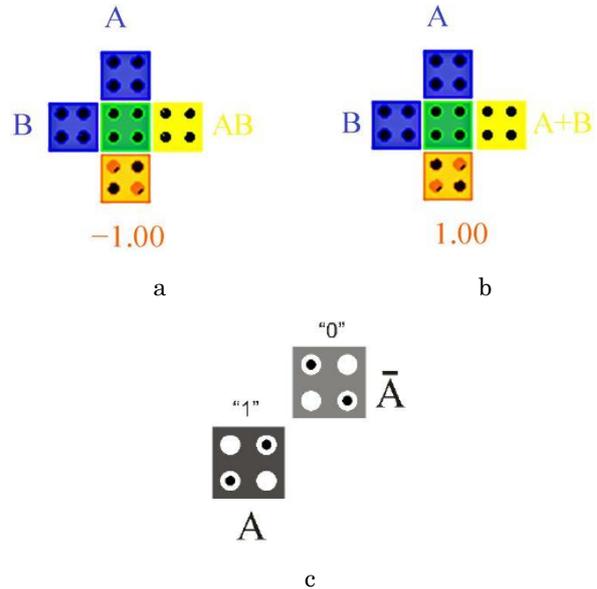


Fig. 4 – The QCA logic gates (a) AND gate (b) OR gate (c) Inverter gate [2, 8]

2.4 The QCA Comparator

Comparators are used in the CPUs and microcontrollers. The comparator is a hardware electronic device that takes two integers as inputs in the binary form and determines whether one integer is greater than, less than or equal to another integer (A > B, A < B and A = B) [16, 17]. The truth table for the 1-bit comparator is shown in Table 1.

Table 1 – Truth table for 1 bit comparator

A	B	L (A < B)	E (A = B)	G (A > B)
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

In this table, when AB = 00 & 11, both inputs are equal. Therefore, the output E, which is used to denote the state of A = B, will be high. When AB = 01, B is greater than A. Hence, the output L, which is used to denote the state of B > A, is active, and when AB = 10, A is greater than B. So, the output G, which is used to denote the state of A > B, is active.

From the truth table, the logical expressions for each output can be expressed as follows:

$$\text{If } A < B \text{ then } L = \bar{A}B \quad (3)$$

$$\text{If } A = B \text{ then } E = \bar{A}\bar{B} + AB \quad (4)$$

$$\text{If } A > B \text{ then } G = A\bar{B} \quad (5)$$

There are many attempts to improve the performance of the QCA comparator such as [5, 6, 8, 9]. In

the rest of this section, the previous designs are presented and reviewed.

In [5], a 1-bit comparator with 100 cells have been designed. This circuit is divided into four parts. For stable information transmission, this circuit is connected to four different clock zones.

The designed comparator in [6] has three outputs. This comparator composed of two layers with 79 cells. For an  $n$ -bit full comparator, the output E of one stage is fed directly to the input of the next stage.

The comparator in [8] has been designed with 73 cells. This comparator has two inputs and three outputs. These two inputs are compared and then the results are sent to one of three outputs.

In [9], a comparator with three input has been designed. The two 5-outputs majority gates generate L and G at the same time and the 3-input majority gate generates E after 0.25 clock cycles delay. This architecture uses 43 cells and occupied area is  $0.06 \mu\text{m}^2$ .

### 3. THE PROPOSED QCA COMPARATOR

In this paper, we rewrite the equations 3-5 as follows:

$$\text{If } A < B \text{ then } L = \bar{A}B = \text{Maj}(\bar{A}, B, 0). \quad (6)$$

$$\text{If } A > B \text{ then } G = A\bar{B} = \text{Maj}(A, \bar{B}, 0). \quad (7)$$

$$\text{If } A = B \text{ then } E = \bar{A}\bar{B} + AB, \quad (8)$$

$$E = \text{Maj}(\text{Maj}(\bar{A}, \bar{B}, 0), \text{Maj}(A, B, 0), 0) \\ \bar{\text{Maj}}(L, G, 0).$$

In this section, we propose new and efficient QCA comparator based on these equations. The proposed QCA comparator architecture is shown in Figure 5.

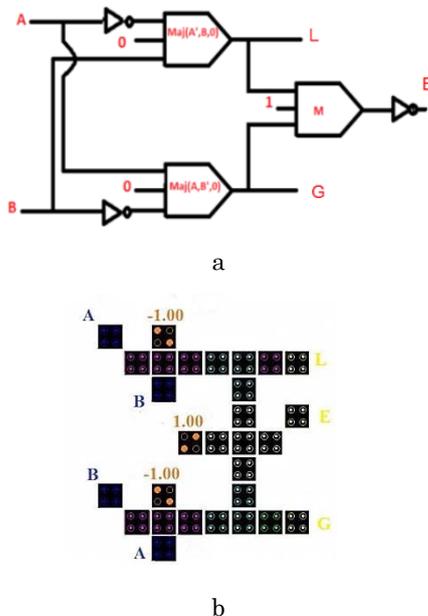


Fig. 5 – The proposed QCA comparator (a) logic circuit, (b) layout

As it is shown in Figure 5, the proposed comparator

is composed of three majority gates. Two 3-input majority gates generate G ( $A > B$ ) and L ( $A < B$ ). The outputs of these 3-input majority gates, act as inputs for 3-input majority gate and generate E ( $A = B$ ). When A and B are equal, the output  $A = B$  is 1. If A is greater than B, the output G is 1 and if A is smaller than B, the output L is 1.

### 4. SIMULATION RESULTS AND COMPARISONS

The proposed QCA comparator architecture is simulated using QCADesigner tool version 2.0.3. Table 2 shows the utilized parameters for the simulation.

Table 2 – The utilized parameter for the simulation of the proposed comparator architecture

Parameter	Value
Number of samples	12800
convergence tolerance	0.001000
radius of effect [nm]	65.000000
relative permittivity	12.900000
clock high	$9.800000e^{-22}$
cell size [nm]	$18 \times 18$
clock low	$3.800000e^{-23}$
cell distance [nm]	2
clock amplitude factor	2.000000
layer separation	11.500000
maximum iterations per sample	100
the diameter of the quantum dot [nm]	5

These simulation results demonstrate that the proposed QCA comparator has correct logic function. In addition, the designed comparator has 29 cells and the area occupied by circuit is  $0.04 \mu\text{m}^2$ .

Table 3 summarizes the simulation results of the proposed QCA comparator architecture in comparison with other QCA comparator architectures in [5, 6, 8-10].

Table 3 – Comparison of the QCA comparators

Reference	Number of cells	Area (in $\mu\text{m}^2$ )	Delay
[5]	100	0.13	1
[6]	79	0.03	1
[8]	73	0.06	1
[9]	43	0.06	1.25
[10]	81	0.06	0.75
This paper	29	0.04	1

Based on these simulation results, the proposed comparator has advantages in terms of the number of required cells in comparison with other QCA comparator architectures in [5, 6, 8-10].

### 5. CONCLUSION

The QCA technology is a promising and helpful technology for circuit design at nano scale. In this paper, a new architecture has been proposed for the QCA

comparator. The performance of the proposed QCA comparator has been verified using QCA Designer tool version 2.0.3. The simulation results showed that the number of required cells in the proposed QCA comparator is 29 cells and the occupied area by the proposed QCA comparator architecture is  $0.04 \mu\text{m}^2$ . In comparison with the previous comparator architecture, the

proposed QCA comparator architecture achieved 36% reduction in terms of the number of required cells. Therefore, the proposed QCA comparator architecture has a huge potential to be an efficient architecture for hardware implementation of comparators in nano technology.

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