JOURNAL OF NANO- AND ELECTRONIC PHYSICS
Vol. 5 No 4, 04054(3pp) (2013)
ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ
Том 5 № 4, 04054(3cc) (2013)

Modeling of Field Effect Mobility Using Grain Boundaries on Nanocrystalline Silicon Thin-Film Transistor (nc-Si TFT)

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(Received 19 July 2013; published online 31 January 2014)

This work presents the effect of grain boundaries in nanocrystalline silicon thin-film transistors (nc-Si TFT). In this study, it is assumed that the nanocrystalline silicon film which is used as the channel material in TFT consists of grain boundaries perpendicular as well as parallel to the carrier flow. Analytical model for mobility due to perpendicular GBs (μ_{perp}) and mobility due to parallel GBs ($\mu_{parallel}$) are developed separately and then the overall (effective) mobility, μ_{FE}, is calculated incorporating both type of GBs. Thereafter the overall (effective) mobility μ_{FE} and drain current are plotted as a function of gate voltage. The trend observed from the theoretical plot of drain current versus gate voltage is in agreement with the experimentally observed trend.

Keywords: Grain boundaries, Nanocrystalline silicon, TFT.

PACS number: 85.30.De

1. INTRODUCTION

High field effect mobility thin film transistors find immense application in active matrix liquid crystal display (AMLCD) or active matrix organic light emitting diode (AMOLED) displays [1], [2]. Amorphous silicon is easily deposited over large areas at low deposition temperatures (below 450 °C) but it suffers degradation under bias stress and under illumination. To avoid this problem, amorphous silicon is converted to polycrystalline silicon using high temperature thermal annealing. Polycrystalline silicon is more stable but its fabrication requires expensive substrates due to high temperature processes. Nanocrystalline silicon has properties in between amorphous and polycrystalline silicon. Low temperature (below 150 ºC) deposition techniques have been proposed [3] for nanocrystalline silicon. At the same time, nanocrystalline silicon is much more stable than amorphous silicon due to a lower density of states. Thus by combining the advantages of both amorphous and polycrystalline silicon, nanocrystalline silicon becomes extremely well suited for fabrication of thin film transistors for the applications described earlier.

The effect of grain boundaries (GBs) on the carrier transport of polycrystalline silicon TFT have been discussed by various researchers [4-6], but the effect of GBs on nc-Si TFT were hardly reported [7].

This paper is organized as follows: In section 2, the modeling of transverse (perpendicular) and longitudinal (parallel) GBs are reported. Section 3 provides the results and discussion based on the developed model. The last section, section 4 concludes the study given in the paper.

2. THEORY AND MODEL

Figure 1 shows the perpendicular grain boundaries as well as the energy band diagram along the length of the channel of an enhancement type n-channel device (p-substrate). In the figure D_G is the grain size, D_{GB} is the size of the grain boundary, D_d is the width of the depletion region ($D_{GB} << D_G$). The grain boundaries contain trap states which trap electrons, thereby leading to a reduction in effective hole concentration in the grain boundaries. Difference in hole concentration between the bulk and the grain boundaries leads to band bending at the grain boundaries. Ψ_B represents the amount of band bending at the grain boundary.

Let $R_{G,\,perp}$ represent the resistance of a single grain, $R_{GB,\,perp}$ represent the resistance of a grain boundary, $n_{g,\,perp}$ represent the number of grains.

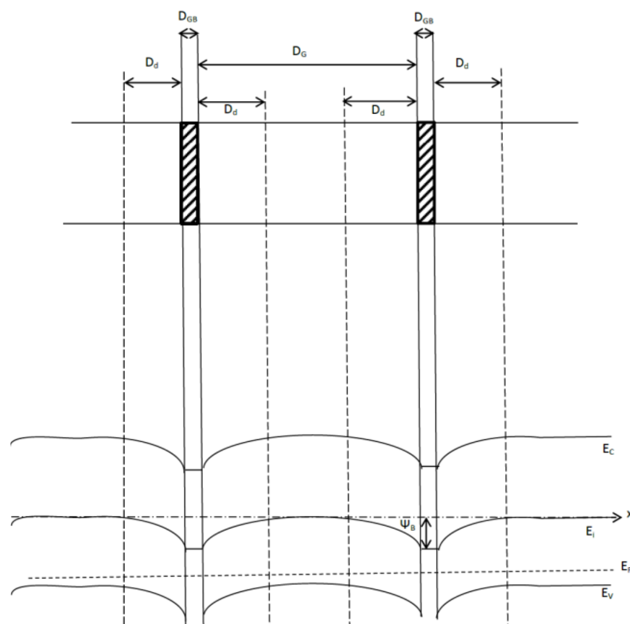

Fig. 1 – (Top) Cross-section in presence of perpendicular (transverse) grain boundary. The shaded regions represent the grain boundaries. (Bottom) Energy band diagram along the length of the nanocrystalline silicon film

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Assuming that the grains and grain boundaries together form a series combination of resistances along the channel from source to drain, the total channel resistance $R_{T,\,perp}$ is given by

$$R_{T,\,perp} = n_{g,\,perp}\, R_{G,\,perp} + (n_{g,\,perp} - 1)\, R_{GB,\,perp} \quad (1)$$

where, $n_{g,\,perp} = D / D_G$ approximately, considering that $D_{GB} << D_G$.

$$R_{T,\,perp} = \frac{D}{A\sigma_{eff,perp}},\; R_{G,\,perp} = \frac{D_G}{A\sigma_G},\; R_{GB,\,perp} = \frac{D_{GB}}{A\sigma_{GB}}$$

Substituting these values in eq. (1),

$$\frac{D}{A\sigma_{eff,perp}} = \frac{n_{g.perp}D_G}{A\sigma_G} + \frac{(n_{g.perp.}-1)D_{GB}}{A\sigma_{GB}} \quad (2)$$

Let N be the hole concentration in the bulk of the grain.

$\sigma_{eff,perp} = qN\mu_{perp}$ and $\sigma_G = qN\mu_G$

$\sigma_{GB} = (q\mu_{GB})p$, where 'p' is the hole concentration in the GBs

$$\begin{aligned}\sigma_{GB} &= (q\mu_{GB})n_i\exp((E_i - E_F)_{\mathrm{GB}} / kT)\\ &= (q\mu_{GB})n_i\exp(((E_i - E_F)_{\mathrm{bulk}} - q\Psi_B) / kT)\\ &= (q\mu_{GB})n_i\exp((E_i - E_F)_{\mathrm{bulk}} / kT)\exp(- q\Psi_B / kT)\\ &= (q\mu_{GB})N\exp(- q\Psi_B / kT) \quad (3)\end{aligned}$$

[Taking $n_i\exp((E_i - E_F)_{\mathrm{bulk}}) / kT) = N$, the hole concentration in the bulk of the grain. n_i is the intrinsic carrier concentration].
where μ_G and μ_{GB} represent the mobility of the grain and grain boundaries respectively and σ_G and σ_{GB} represent the conductivity of the grain and grain boundaries respectively.

Now eq. (2) becomes,

$$\frac{n_{g,perp}D_G}{AqN\mu_{perp}} = \frac{n_{g,perp}D_G}{AqN\mu_G} + \frac{(n_{g,perp}-1)D_{GB}}{AqN\mu_{GB}\exp\left(-\dfrac{q\Psi_B}{kT}\right)} \quad (4)$$

Solving eq. (4) for μ_{perp} we get

$$\mu_{perp} = \frac{\mu_G}{1+\left[\dfrac{\left(n_{g,perp}-1\right)\mu_G D_{GB}}{n_{g,perp}\mu_{GB}D_G}\right]\exp\left(\dfrac{q\Psi_B}{kT}\right)} \quad (5)$$

where the potential barrier height is related to the gate voltage by [4]

$$\Psi_B = \frac{q^2 N_T{}^2 t_{si}}{8\varepsilon_s C_{ox}(V_G - V_T)} \quad (6)$$

where N_T is the trap state density and t_{si} is the thickness of the nano crystalline silicon film, ε_s is the permittivity of silicon, C_{ox} is the oxide capacitance per unit area.

Now assuming that channel also consists of parallel (longitudinal) GBs which are shown in figure 2. Assuming that t_G is the thickness of a single grain and t_{GB} is the thickness of a grain boundary. As in the case of perpendicular GBs, the trapping of electrons at GBs leads to reduction of hole concentration in the GBs, resulting in band bending at the grain boundaries. It is assumed that the extent of band bending at the GBs (Ψ_B) is the same as in the perpendicular case.

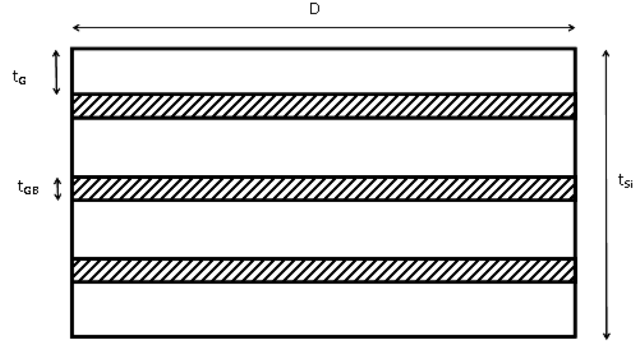

Fig. 2 – Channel in presence of parallel (longitudinal) grain boundaries. The shaded regions represent the grain boundaries

It is clear from figure 2, that the grains and grain boundaries form a parallel combination of resistances. Hence the equivalent resistance of the entire film can be written as

$$\frac{1}{R_{T,parallel}} = \frac{n_{g,parallel}}{R_{G,parallel}} + \frac{\left(n_{g,parallel}-1\right)}{R_{GB,parallel}} \quad (7)$$

which gives the parallel mobility as

$$\mu_{parallel} = \frac{\mu_G t_G}{t_G + \left(1-\dfrac{1}{n_{g,parallel}}\right)t_{GB}} + \frac{\mu_{GB}t_{GB}\exp\left(-\dfrac{q\Psi_B}{kT}\right)}{t_{GB} + \dfrac{t_G}{\left(1-\dfrac{1}{n_{g,parallel}}\right)}} \quad (8)$$

The effective field effect mobility (μ_{FE}) can be obtained from the following relation

$$\frac{1}{\mu_{FE}} = \frac{1}{\mu_{perp}} + \frac{1}{\mu_{parallel}} \quad (9)$$

The mobility (μ_{FE}) calculated by the above model is used to calculate the drain current in saturation using the equation

$$I_D = \frac{\mu_{FE}C_{ox}Z}{2D}\left(V_G - V_T\right)^2 \quad (10)$$

3. RESULTS AND DISCUSSION

Table 1 shows the typical values of the model parameters used in the calculations [8]. Figure 3 and 4 illustrate the calculated values of effective field effect mobility and drain current as a function of gate voltage at room temperature. It is observed that effective field effect mobility and hence the drain current increases rapidly with the increase in gate voltage which is due to the gate-induced barrier lowering effects. Also as N increases, barrier potential will de-

crease. This means that available carriers for transport will increase hence it decreases the trap states at the oxide-silicon interface of nc-Si TFT. This effect results in an increase in the channel mobility which in turn increases the drain current.

Figure 5 shows the experimental values of drain current versus gate voltage taken from Teng and Anderson [8] in saturation region and at a drain voltage, $V_D = 9$ V.

Table 1 – Parameters used in the study [8]

Parameters	Values
D_{GB} / D_G	0.1
t_{GB} / t_G	0.1
μ_G	203 cm^2/V-s
μ_{GB}	0.3 cm^2/V-s
t_{Si}	90 nm
D_G	25 nm
t_G	25 nm
Z / D	200 μm / 25 μm
t_{ox}	150 nm
V_T	3 V

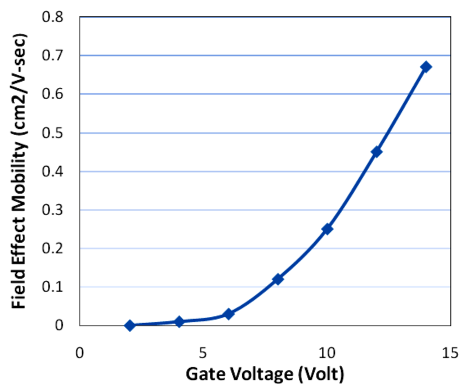

Fig. 3 – Computed variation of field effect mobility with gate voltage at room temperature

It is observed that the trend of the experimental values are same as that of the computed values using developed analytical model, however the deviation from the actual values are attributed due to the fact that the actual device may have affected from various other effects such as channel length modulation, drain induced barrier lowering and impact ionization which may be further incorporated to strengthen the present model.

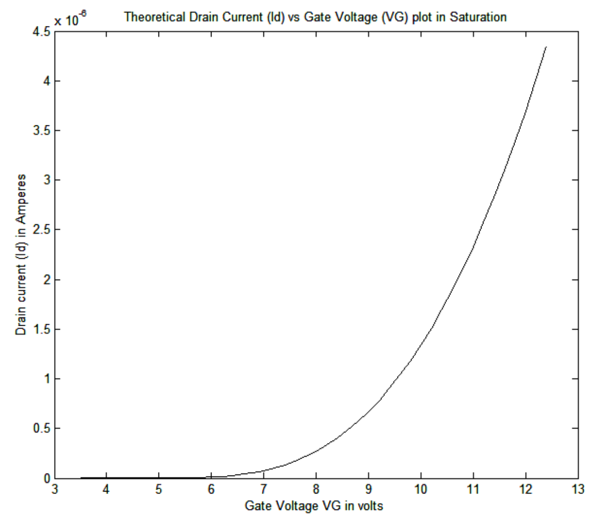

Fig. 4 – Computed variation of drain current with gate voltage at room temperature

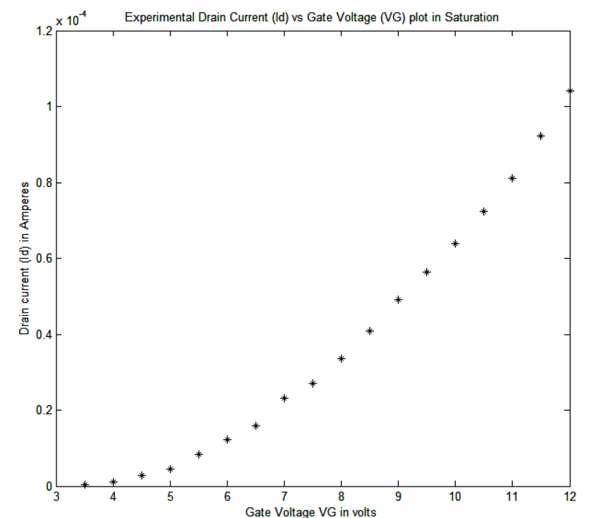

Fig. 5 – Experimental variation of drain current with gate voltage at room temperature [8]

4. CONCLUSION

This work proposed the development of an analytical mobility model for nanocrystalline silicon thin film transistors considering the effects of perpendicular and parallel GBs. The mobility is then used to calculate the drain current. The trend obtained is in agreement with the experimentally observed trend.

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