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Prospects of III-Vs for Logic Applications

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The increasing challenges for further scaling down of Si CMOS require the study of alternative channel materials. This paper highlights the significance of III-V compound semiconductor materials in order to face the looming fate of Si CMOS technology. The potential advantages of using III-Vs as channel materials for future III-V CMOS is its outstanding transport properties that have been widely accepted in high frequency RF applications. However, many significant challenges in front of III-V digital technology needs to be overcome before III-V CMOS becomes feasible for next generation high speed and low power logic applications. But it may be that this situation is changing given recent progress in the fabrication of high-mobility III-Vs based heterostructure electronic devices for logic applications to fulfill the needs towards the everyday evolving III-V CMOS technology.

Keywords: CMOS, III-V Materials, HEMT, Logic, Digital.

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1. INTRODUCTION

Silicon CMOS for several decades has remained the undisputed technology for digital applications due to its scalability and high switching speed. It has been forecasted that the scaling limit of silicon CMOS would reach an ultimate limit of 10 nm physical gate length around the year 2014[1]. Therefore it has become a primary interest for both academy and industry to find suitable alternatives to sustain the scaling trend which is the backbone of CMOS technology. In this regard, ITRS Emerging Research Devices (ERD) and Emerging Research Materials (ERM) have also been considering for other technologically feasible solutions for scaling CMOS to and beyond the 16 nm technology generation by replacing silicon with other semiconductor channel materials and identifying new logic devices and architectures [2]. The material properties that are considered for 'More Moore' logic applications are high carrier mobility, high peak saturation velocity, low operating voltages and scalability, yet compatible with the present day CMOS technology. Although, carbon nanotubes and semiconductor nanowires like GaN and Si are being considered as next generation materials [1], they are not yet tested with time for a real device technology. In this regard, III-V semiconductors are attractive as alternative channel materials for future digital applications. This is however not the first instance for III-V materials being considered for digital applications. In 1981, for the first time, 1.7 μm-gate enhancement-mode and depletion-mode HEMTs ring oscillators had been realized with switching delay of 56.5 ps at room temperature [3]. The ultra high speed HEMTs also played important role in supercomputer systems. Seymour Cray, recognized as the 'father of supercomputing' explored, for the first time, GaAs for logic circuits in CRAY-3 system [4]. However, this technology, due to cost and complexity, could not sustain itself in the area of digital applications and was commercialized for RF applications [5]. Although digital III-V have revived from the past debacle, there are still many challenges that need to be overcome in material and device technology for high speed digital applications. There has been a considerable effort by academy and industry to understand and face these technological barriers and use III-V for applications in low power and high speed digital devices.

This paper reviews the prospects of III-V materials and devices contributing to the body of knowledge of future high speed digital applications.

2. III-V CHANNEL MATERIALS FOR LOGIC APPLICATIONS

III-V materials, particularly, InGaAs, InAs, InSb have superior electronic properties that make them promising candidates for low noise, low power, and high speed digital applications. A way forward in 'More Moore' diversification is the use of these materials as channel in digital devices due to their proven record in various high frequency applications, and well established and matured technology next to silicon. The flexibility of these materials allows quantum well engineering by channel quantization techniques[6], strain engineering[7] and band gap engineering which can be utilized to obtain better logic performance.

The channel material properties like high mobility and saturation velocity determine important device metrics relevant to logic applications like drain induced barrier lowering (DIBL), ON current, OFF current, logic delay, operating voltage, and sub-threshold slope. Consequently, InGaAs has emerged as an important material for digital applications. Another advantage of this material is that it can be enriched with InAs to yield better mobility and peak saturation velocity. This improves the cutoff frequencies and increases the ON current. Furthermore, following the path of present day silicon architecture, InGaAs can also be strained engineered to increase its mobility [7].

Another attractive material from the III-V family that promises high speed and low power logic application is InAs. InAs features electron mobility as high as 33,000 cm^2/V-s. This outstanding material can be used as composite channels for digital applications.

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The determinants of III-V logic applications can be further improved by using InSb which has the highest electron mobility and saturation velocity among all the semiconductors. Also, the high hole mobility of InSb can be utilized in p-channel III-V logic applications. Strain engineering the InSb channel can further improve the hole mobility.

Although GaN has been used for high power applications, it seems to offer optimistic solution to Si roadmap challenges, despite the fact that GaN has low electron mobility. The optimism is because of GaN's high bandgap which minimizes the risk of high OFF leakage current. Furthermore, the high polarization electron density combined with high carrier confinement in the GaN/AlGaN heterojunction provides higher drain current. These favorable electronic properties enhance the I_{ON}/I_{OFF} ratio. Properties like high thermal stability, large bandgap, and ability to withstand heavy doses of radiation makes GaN based digital electronics compatible for high temperature operations like oil extraction, electronics for geothermal energy, spacecrafts and other harsh environments [8]. Hence, GaN can be considered as a prospective material in III-V digital family.

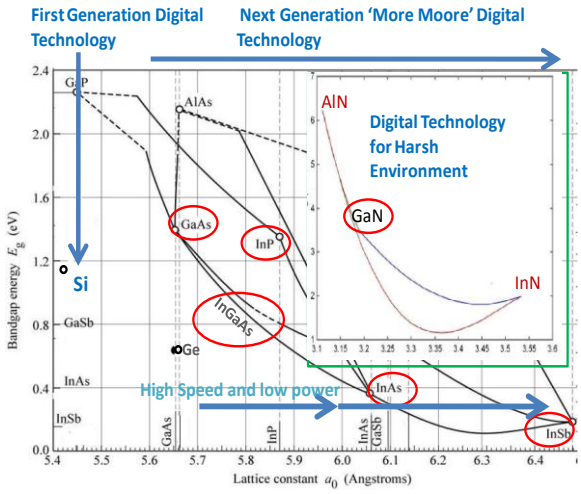

Fig. 1 – Materials for 'More Moore' Diversification towards III-V logic applications

Another material property that needs to be considered for this family of semiconductors is the T-L separation in III-V materials. The T-L separation determines ballistic transport and valley scattering and affects important logic determinants like DIBL and subthreshold slope [9].

Table 1 shows a comparative study of electron and hole motilities, peak saturation velocity, T-L valley separation, and bandgap of typical III-V materials that can be used for logic applications taking Si and Ge as reference materials [10], [11].

3. CHALLENGES OF III-V CHANNEL MATERIALS AND DEVICE TECHNOLOGY FOR LOGIC APPLICATIONS

One of the greatest challenges to use InGaAs, InAs and InSb as channel materials is the high leakage current because of its low bandgap. There is a general trend that impact ionization rate increases with decreasing bandgap. This decrease in bandgap causes kink effect and excess gate leakage current due to impact ionization [12]. The schottky gate leakage increases the OFF current and hence reduces the I_{ON}/I_{OFF} figure of merit [13]. In contrast, GaN has higher bandgap and therefore lower leakage current. However, a possible trade-off of GaN is its low mobility as compared to other digital III-V materials.

Digital applications require low leakage current when the gate voltage is off. Therefore, enhancement-mode devices are favourable for logic applications. However, it has been observed that as vertical scaling of the barrier is performed to achieve E-mode, gate leakage current increases and thereby I_{OFF} increases [13]. Although, thinning of the barrier is necessary to maintain proper aspect ratio during gate length scaling, it is obtained at the cost of high leakage current. To alleviate this problem, a high-k dielectric compatible with III-V is necessary. This requires identifying dielectric materials with suitable III-V/dielectric interface quality and low equivalent oxide thickness [14] which is a challenge in itself.

It is evident from Table 1 that there is a soaring imbalance between III-V hole mobility and electron mobility. The challenge here lies in the improvement of hole mobility of III-V p- channel materials in order to have a compatible device footprint and speed with respect to n-channel.

Also, the success of III-V materials in RF applications is much attributed to the recessed gate etch technology. In contrast, the recessed gate etch technology is not well suited for logic applications due to its large device footprint. Hence, self-aligned gate technology must be adopted for III-V logic applications [13]. However III-V can be used effectively in LSI and VLSI applications compromising the low packing density with high speed.

Last, but certainly not least, are the issues related to integration of III-V materials on silicon substrates for future logic applications. III-Vs on Si render cost-effective manufacturing, flexible wafer size, high thermal conductivity and use of matured technology. The challenge here lies in reducing lattice mismatch, anti-phase domains and thermal coefficient mismatch to produce high quality, crack-free active layers. Also the crystal orientation would be an important factor as Si CMOS is based on advantageous (001) orientation. This would probably require the growth of III-V on this orientation substrate because of the ease in processing and maturity in technology.

4. PRESENT STATUS OF LOGIC DEVICES USING III-V MATERIALS

Although III-V devices is not the first choice for logic applications, High Electron Mobility Transistors (HEMT) has served as an excellent model for investgating the logic characteristics of III-V materials [14]. Recently there has been large number of experimental analysis of InGaAs HEMTs on lattice matched InP substrates for future logic applications. Figures of merit significant to logic applications, such as logic gate delay, I_{ON}/I_{OFF}, Drain-Induced Barrier Lowering (DIBL)

Table 1– Relevant properties of III-V materials for digital applications

Materials	Electron mobility ($cm^2V^{-1}s^{-1}$)	Electron saturation velocity (cms^{-1})	Hole mobility ($cm^2V^{-1}s^{-1}$)	Hole saturation velocity (cms^{-1})	T-L Separation (eV)	Bandgap (eV)
$In_{0.53}Ga_{0.47}As$	14000	3.0×10^7	400	0.40×10^7	0.55	0.80
InAs	33000	3.5×10^7	460	0.50×10^7	0.90	0.36
InSb	77000	5.0×10^7	850	0.80×10^7	0.51	0.17
GaN	< 1000	1.4×10^7	< 200	–	1.1 – 1.9	3.39
Si	1350	1.0×10^7	460	0.72×10^7	-	1.12
Ge	3900	0.7×10^7	1900	0.63×10^7	-	0.66

and sub- threshold slope (S) have been evaluated and have shown comparable results with silicon MOSFETs [16].Along with this, the experimental investigation of scaling of InGaAs FET on InP substrate [17] and numerical drift–diffusion simulation [18] have provided sufficient evidence for these devices to be ideal for future high speed, low power logic applications. Moreover, much progress has been made in realizing InGaAs enhancement -mode FETs and its integration on silicon substrate using metamorphic buffer layers. The use of (100) crystal orientation substrate has made these devices compatible with present day mainstream CMOS technology. Though this device has been fabricated using recessed gate etch technology, it has shown impressive logic characteristics [19].Self-aligned enhancement-mode InGaAs HEMT, compatible for VLSI applications, has been demonstrated by N.Waldron et.al. In this work, design elements for technology were determined which can serve as a self-aligned implementation model in digital III-Vs [13].

The logic performance of InAs with 40 nm gate length has been investigated using composite channel on InP substrate. On optimizing the thickness of the channel and scaling the gate length from 340 nm to 40 nm, constant threshold voltage and high transconductance have been achieved. In comparison to InGaAs, InAs HEMTs have shown better logic characteristics which can be attributed to its high mobility. Also, InAs HEMT has shown superior DIBL and sub-threshold swing as compared to Si NMOSFET [20].A prerequisite step of heterogeneous integration of InAs channel on Si substrate has been demonstrated using two buffer layers [21].This could pave the way for future high speed logic applications using InAs on Si platform.

T. Ashley et.al reported for the first time 0.2 µm gate length InSb quantum well field-effect transistors (QWFET) for digital applications. Benchmarking against Si MOSFET suggested that InSb-based QWFETs could achieve comparable high speed performance and lower power dissipation [22]. Improvement in the logic performance was obtained when the device was scaled to 85 nm along with the realization of enhancement mode operation. The QWFET when com-compared with Si MOSFETs showed 2.8 times reduction in gate delay and 50% higher cut-off frequency [22]. Since these devices were fabricated on semi-insulating GaAs substrate; it could hinder its hybrid integration with silicon technology. In order to overcome this challenge, InSb quantum well transistor on silicon substrate using intermediate buffer has been confirmed with similar logic performance as achieved on GaAs substrate [24].

It can be appreciated that the III-V digital devices have been operated efficiently at a low supply voltage of 0.5 V and have shown better performance in the logic metrics compared to state-of-art Si MOSFETs. The low supply voltage suggests that future III-V CMOS will use low power, run cooler and faster than its silicon-based counterpart.

The application of logic devices is not limited to room temperature and favorable environment. In order to meet the challenges of digital applications in high temperature and harsh environment, researchers have come up with digital circuits using GaN HEMTs. T. Hussain et.al demonstrated 31-stage ring oscillators and comparator circuit as illustrated in Fig. 2 and Fig. 3 respectively.

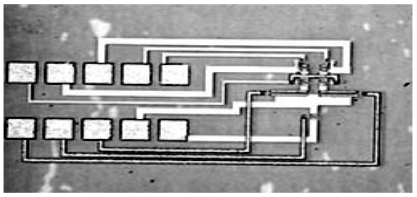

Fig. 2 – GaN HEMT comparator circuit [25]

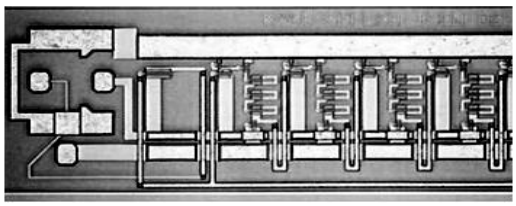

Fig. 3 – A portion of 31-stage ring oscillator [26]

In addition to this, integrated enhancement and depletion mode (E/D) GaN HEMT has been fabricated and divide-by-two circuit and ring oscillator implemented with this technology [27]. GaN digital technology should have the potential to operate in environments where silicon technology would not suffice.

Benchmarking against the silicon CMOS, Table 2 provides a comparative study of logic parameters of various III-V devices.

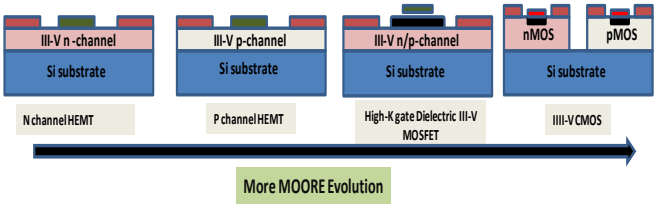

Fig. 4 – Transition from III-V HEMT model towards future III-V CMOS

Table 2 – Comparison of logic characteristics of III-V devices

Channel	Substrate	Gate length (nm)	Device	DIBL (mV/V)	*S* (mV/dec)	I_{ON}/I_{OFF}	Supply voltage (V)	Ref.
InGaAs	InP	60	HEMT	93	88	1.6×10^4	0.5	[17]
InGaAs	Si	80	QWFET	150	155	~ 2150[18]	0.5	[28]
InAs	InP	40	HEMT	72	72	2.5×10^4	0.5	[29]
InSb	GaAs	85	QWFET	95	105	330	0.5	[23]
InSb	Si	85	QWFET	94	82	370	0.5	[24]
GaN	-	500	HEMT	100	150-250	$> 10^4$	-	[8]
Si	-	55	CMOS	80	90	0.5×10^3	0.5	[10]

While III-Vs have impressive performance for n-channel digital applications, the p-channel HEMTs tend to lag behind.

As seen from Table 1, InSb is a promising p-channel material due to its high mobility which can be further enhanced by strain. M. Radosavljevic et. al has demonstrated 1.9 % compressively strained InSb channel. The compressive strain increases the mobility and a high hole mobility of 1,230 cm^2/V-s has been recorded. Benchmarking against Si MOSFET showed that p-channel InSb-based QWFETs shows approximately two times higher speed at matched power [30]. Another research group has presented InGaSb p-channel HFETs with an InAlSb barrier layer. In this work, hole mobility of 1,500 cm^2/V-s was achieved using a biaxial compressive strain of 2 % [31].

With impressive performance of both p-channel and n-channel HEMTs, the transition of III-V digital devices from the HEMT model to a realistic III-V CMOS would be possible with an effective gate stack solution. The evolution of HEMTs to III-V MOSFETs using various high-k gate dielectrics has been reviewed elsewhere [32].

As the improvement in III-V device and material technology continues, another mile stone that needs to be achieved is the integration of the p-channel and n-channel FETs for next generation III-V CMOS.

Recently, researchers in AIST along with University of Tokyo, Sumitomo Chemical, and NIMS have successfully demonstrated the first III-V/Ge CMOS integrated by wafer bonding technique on Ge substrate with 200 % enhanced mobility as compared to Si CMOS transistors. Although the p-channel FET has been fabricated using non III-V material (Ge), this demonstration suggests an optimistic scenario for a complete next generation III-V CMOS [33] (Fig. 4).

5. CONCLUSION

Due to significant challenges that exist for silicon CMOS technology many potential solutions are being investigated to move towards More Moore devices. The use of III-V materials for logic applications has shown impressive results but many hindrances need to be addressed before it can be completely integrated in next generation III-V CMOS.

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