GERMANIUM NANOCRYSTALS EMBEDDED IN SILICON DIOXIDE FOR FLOATING GATE MEMORY DEVICES

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Metal-oxide-semiconductor (MOS) capacitors with tri-layer structure consisting of rf magnetron sputtered grown germanium (Ge) nanocrystals (NCs) and silicon dioxide (SiO$_2$) layers sandwiched between thermally grown tunnel and sputtered grown cap oxide layers of SiO$_2$ were fabricated on p-Si substrates. Plane view transmission electron micrographs revealed the formation of spherically shaped and uniformly distributed Ge NCs. The optical and electronic characteristics of tri-layer structures were studied through photoluminescence (PL) spectroscopy and capacitance-voltage (C-V) measurements, respectively. Frequency dependent electrical properties of the structures have been studied. The optical emission characteristics support the confinement of the carriers in Ge NCs embedded in oxide matrices. An anticlockwise hysteresis in C-V characteristics suggests electron injection and trapping in Ge NCs.

Keywords: GERMANIUM NANOCRYSTALS, FLOATING GATE MEMORY, METAL-OXIDE-SEMICONDUCTOR, PHOTOLUMINESCENCE SPECTROSCOPY, FLAT BAND VOLTAGE.

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1. INTRODUCTION

Recently, considerable amount of research has been focused on nanocrystals (NCs) floating gate memory (FGM) devices due to their wide applications in the integrated flash memories. Compared to conventional flash memories, NCs FGMs offer smaller operating voltages, lower power, better endurance characteristics, faster write/erase speed, higher retention and scalability [1-4]. The continuous floating gate layers in conventional flash memories are replaced by metal or semiconductor NCs embedded in an oxide layer [1]. Both semiconductor and metal NCs such as Si [5, 6], Ge [1, 4, 7], SiGe [8], Au [9], and Ni [10] are promising candidates for the charge storage nodes in floating gate devices. Due to larger carrier mobility, smaller band-gap and higher excitonic Bohr radius compared to Si, Ge NCs are considered to be ideal nodes for use in MOS compatible memory devices. The change in Gibbs free energy of formation (at 289.15 K) of GeO$_2$ (111.8 kcal/mol) is much smaller than that of SiO$_2$ (204.75 kcal/mol) [11], which is beneficial for the formation of stable Ge nanoparticles [12] in oxide matrices during thermal annealing.

In this article, we report on the emission, charging, discharging and charge-storage characteristics of a tri-layer memory device structure with nanocrystalline Ge embedded in SiO$_2$ matrix. Room temperature photoluminescence (PL) in the visible range from embedded Ge NCs are presented to evident the effect of quantum confinement effect in the Ge NCs.

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2. EXPERIMENTAL

The memory structures used in the study were metal-oxide-semiconductor (MOS) capacitors with a dielectric stack consisting of Ge NCs embedded in oxide matrices, sandwiched between tunneling and capping layers of SiO$_2$. Prior to deposition, Si substrates of p-type (100) orientation, with resistivity of $\sim$14 $\Omega$-cm were cleaned by Piranha solution followed by dipping in 1% hydrofluoric (HF) acid for 1 min to remove the surface native oxide followed by rinsing in de-ionized water and drying in a flux of N$_2$. A tunneling oxide layer of thickness 5-10 nm was first grown on cleaned Si surface in dry oxygen ambient using thermal oxidation at 900 $^\circ$C for 12 min. The intermediate layer was then deposited by radio-frequency (rf) magnetron sputtering from 3 inch diameter n-type Si wafer masked with Ge wafer pieces of defined area in the argon (Ar) and oxygen (O$_2$) mixture in the ratio of 1:2 at a substrate temperature of 200 $^\circ$C. The chamber was first evacuated to a base pressure of $5 \times 10^{-5}$ mbar. The target to substrate distance was kept fixed at 6 cm and the working pressure was maintained at 0.02 mbar. The deposition was carried out at rf power of 75 W for 5 min. Finally, the top capping oxide layer (30-40 nm thick) was deposited by rf sputtering from a SiO$_2$ (99.999% pure) target in an Ar ambient at a substrate temperature of 200 $^\circ$C. The deposition was done for 45 min at a pressure of 0.02 mbar with rf power of 100 W. The tri-layer structures were then subjected to thermal annealing in N$_2$ ambient at two different temperatures 950 $^\circ$C and 900 $^\circ$C for 120 min, respectively. Aluminum (with 1% Si) contacts were then deposited by thermal evaporation on both the front and back surfaces to fabricate MOS capacitors using the Trilayer structure.

The PL spectra of Ge NCs embedded in SiO$_2$ matrix was recorded at room temperature using a He-Cd laser (325 nm) source, a triax 320 monochromator and Hamatsu photomultiplier tube. The electrical properties of the tri-layer structure were studied using Keithley 4200-SCS measurement instrument.

3. RESULTS AND DISCUSSIONS

3.1 Structural properties

The microstructural property of Ge NCs was studied by using plane-view HRTEM. Fig. 1 shows the plane view transmission electron microscopic

![Plane view TEM image of Ge NCs in SiO$_2$ matrix](image)

Fig. 1 – Plane view TEM image of Ge NCs in SiO$_2$ matrix
images of Ge NCs embedded in SiO$_2$ matrix. The Ge NCs were observed to be spherically shaped and uniformly distributed throughout the SiO$_2$ matrix. The average size of the NCs was measured to be 6.5 nm.

### 3.2 Optical Characteristics

The room temperature PL spectra of Ge NCs embedded in SiO$_2$ matrices were shown in Fig. 2. The sample shows a broad luminescence peak around 500 nm. The de-convoluted spectrum in the figure reveals three broad peaks overlapping each other at 449 nm, 501 nm and 587 nm. The peak at 449 nm corresponds to the defect state of Ge-oxide and rest two peaks can be attributed to the size distribution of Ge NCs.

In order to interpret the results quantitatively, we applied a simple confinement model by considering electrons and holes confined independently in quantum dots of radius $R$ [13]

$$E_{nl} = E_g + \frac{\hbar^2}{2\mu_{e-h}} (\alpha_{nl}/R)^2 - 1.786e^2/\kappa R,$$

where the second term represents the kinetic energy of electrons and holes while the last term denotes the Coulomb interaction term. $\mu_{e-h}$ is the reduced mass of excitons, $\kappa$ is the static dielectric constant (for Ge $\kappa = 16.30$). $\alpha_{nl}$ is the eigen-value of the zeroth-order spherical Bessel function ($\alpha_{10} = \frac{2}{\sqrt{3}}$), and the band gap energy of Ge $E_g = 0.66$ eV. Using two major PL peak energies in the above formula, we get the diameter of the NCs to be 6.13 nm and 6.92 nm. This result manifests the origin of luminescence from isolated Ge NCs confined within the high-energy gap SiO$_2$ matrix.

![Deconvoluted PL spectra](image)

*Fig. 2 – Deconvoluted PL spectra of sample Ge/SiO$_2$ on Si sample at 300 K*

### 3.3 Electrical Characteristics

Typical high frequency (1 MHz) C-V characteristics of Al/SiO$_2$/NC-Ge/SiO$_2$/Si MOS capacitors were shown in Fig. 3. The classical operation modes of ideal MOS structures with distinct inversion, depletion and accumulation of carriers are observed clearly in the plot. The flat band
voltages are found to be $-5.03\, V$, $-2.53\, V$ for samples annealed at 900 °C and 950 °C, respectively. The higher negative flat band voltage for the sample annealed at 900 °C is attributed to more oxide charges in the tri-layer structure with lower annealing temperature.

The charge storage characteristics of tri-layer structure incorporating Ge NCs have been studied through the C-V characteristics of MOS capacitors by sweeping the bias voltage from accumulation to depletion and back to accumulation.

Fig. 4 displays the normalized high-frequency (1 MHz) C-V characteristics of rf deposited samples. An anti-clockwise hysteresis characteristic indicates the net electron trapping in the tri-layer. The hysteresis width of the sample annealed at 950 °C is found to be 3.82 V in comparison to that of 10.96 V for the same sample annealed at 900 °C. The increase in hysteresis width, on post-deposition annealing of the sample, which is a figure of merit of stored
charge density is attributed to the improved crystallinity of Ge NCs and reduction of defects/traps. The maximum flat band voltage shift of 3.82 V for sample annealed at 950 °C gives rise to a stored charge density of $0.17 \times 10^{12} \text{cm}^{-2}$. On the other hand a shift of 10.96 V obtained for same sample annealed at 900 °C gives rise to a stored charge density of $1.47 \times 10^{12} \text{cm}^{-2}$, as calculated using [14, 15]

$$N_{\text{charge}} = \frac{C_{\text{ox}} \Delta V_{\text{FB}}}{q t_{\text{ratio}}}$$

(2)

where $C_{\text{ox}}$ is the oxide capacitance and $\Delta V_{\text{FB}}$ is the flat band voltage shift. The factor, $t_{\text{ratio}}$ is the thickness ratio of $(t_{\text{gateox}} + 0.5 D_n) / t_{\text{total}}$. Here, $t_{\text{gateox}}$, $D_n$, and $t_{\text{total}}$ are the thickness of cap gate oxide, NC diameter, and total thickness of MOS structure, respectively.

For a better understanding of the C-V results, the frequency dependent capacitance had been investigated at room temperature. The measurement was carried out for the sample annealed at 900 °C for 2 hr. In frequency dependent measurements, we found similar anti-clockwise C-V hysteresis from 1 MHz to 300 kHz. The hysteresis widths are found to be frequency independent, as shown in Fig. 5. The absence of dispersion or stretching of the C-V characteristics along gate voltage axis attributes the origin of hysteresis to stored charges in NCs rather than contribution from the interface traps.

To study the device stability, we have measured the endurance characteristics in Fig. 6 with −6 V to 10 V sweep voltage. We observed a slight change in the hysteresis only after $10^3$ cycles.

![Fig. 5 – Frequency dependent C-V characteristics of tri-layer MOS device](image)

4. CONCLUSIONS

We have fabricated a Trilayer SiO$_2$/Ge-NCs-embedded SiO$_2$/SiO$_2$ sandwiched memory structure using rf magnetron sputtering. The formation of spherically shaped NCs of diameter 6.5 nm has been observed from TEM micrographs. The appearance of strong and broad visible PL at room temperature is due to the quantum confinement of carriers in Ge NCs.
having a distribution of crystallite sizes. The observed shift in flat band voltage in C-V curve has been attributed to electron trapping in Ge NCs. Good endurance characteristics are observed in Ge NCs annealed under an optimum condition.

REFERENCES