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TWO-DIMENSIONAL ANALYTICAL MODELING OF THRESHOLD VOLTAGE OF DOPED SHORT-CHANNEL TRIPLE-MATERIAL DOUBLE-GATE (TM-DG) MOSFET'S

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In this paper, a short-channel threshold voltage model is presented for triple-material double-gate(TM-DG) MOSFET with uniform doping profile in the channel region. To obtain the channel potential expression, the two-dimensional (2D) Poisson's equation has been solved using the parabolic potential approximation with suitable boundary conditions. Subsequently, the surface potential expression has been employed to derive an analytical expression of thresholod. The threshold voltage variation with various device parameters has been shown. To validate the model, ATLAS^{TM} based numerical simulation results have been used.

Keywords: *DG MOSFET, SURFACE POTENTIAL, THRESHOLD VOLTAGE, PARABOLIC APPROXIMATION, ATLAS.*

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1. INTRODUCTION

The ongoing era of CMOS technology, currently heading towards 22nm regime, is gradually centering on multiple-gate MOS structures as single gate MOS devices are found incompetent to overcome the challenges of short-channel effects [1]. In fact, for the increased charge sharing from the source/drain region at shorter channel length, the gate looses its controllability over the depletion region which in turn makes the absolute value of threshold voltage smaller. From this point of view, among different multiple gate structures, double-gate (DG) MOSFETs have drawn potential interests of researchers due to its better scalability [2-5].

Nowadays, multi-material gate structures, like double-material-gate (DMG), offer an alternative way of suppressing SCEs and to increase the average electron velocity along the channel by employing the threshold voltage modulation technique [6]. The threshold voltage modulation is produced by choosing the gate composed of two materials with different work functions ($\varphi_{M1} > \varphi_{M2}$) to introduce a potential step in the channel region which results in higher threshold voltage towards the source and lower threshold voltage towards the drain end [6]. In this way, the gate with lower work function works as screen gate and shields the control gate (with higher work function) by absorbing any detrimental drain-to-source voltage variation.

In an attempt, Long et al [7]. reported that with the introduction of a step in the channel potential double-material gated structures are able to suppress the SCEs like hot-carrier effects and provides better transconductance as well. Afterwards, a Chaudhry et al. [8], presented a simulation based study

of DMG SOI devices. Reddy and Kumar [9] proposed a dual-material double-gate MOSFET in order to incorporate the virtues of single-material DG MOSFETs and dual-material SOI MOSFETs. Razavi et al. [10] reported a simulation based study of TM-DG MOSFET in which it was shown that triple-material is superior to dual-material gate device in suppressing hot-carrier effects (HCEs). Recently, Tiwari et al. [11]. have presented an analytical threshold voltage model for TM-DG MOSFET with light channel doping. However, the authors have not investigated the effect of channel doping on the threshold voltage.

In this paper, an analytical threshold voltage model has been presented for doped channel triple-material short-channel DG MOSFETs. The two-dimensional Poisson's equation has been solved using parabolic potential approximation method [12]. Since the model is developed for heavily doped DG MOS devices, the conventional definition of threshold voltage (gate voltage at which minimum surface potential becomes twice of Fermi potential i.e. $\psi_{s\,min} = 2\Phi_F$) has been utilized. The effect of variation of device parameters on threshold voltage has been demonstrated. The model results have been compared with ATLAS simulation results for validation [13].

2. ANALYTICAL MODELING

2.1 Channel Potential Formulation

The schematic structure of the TM-DG MOSFET device used for our analysis and simulation is shown in Fig. 1 where L, t_{si} and t_{ox} are the gate-length, channel thickness and gate-oxide thickness respectively. The channel has been divided into three regions namely region-I, region-II and region-III with uniform channel doping, N_a, as shown in the figure.

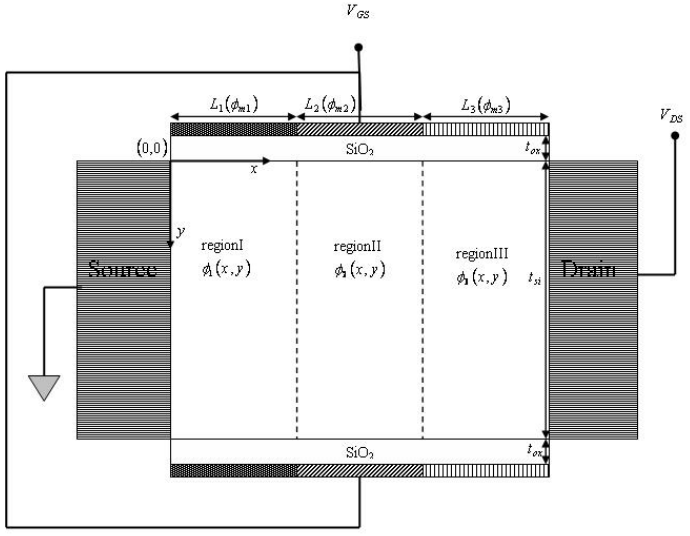

Fig. 1 *– Schematic structure of triple-material double-gate MOSFET*

The front and back gate electrodes of a symmetric TM-DG MOSFET structure are made of three different gate materials with work functions

φ_{m1}, φ_{m2} and φ_{m3} deposited over respective lengths L_1, L_2 and L_3 on the gate oxide layers where $\varphi_{m1} > \varphi_{m2} > \varphi_{m3}$ and $L = L_1 + L_2 + L_3$. Thus, the portion of gate near source end with the highest work function (φ_{m1}) is called the control gate, the middle portion of gate with intermediate work function (φ_{m2}) is named as the first screen gate and the remaining part with the lowest work function (φ_{m3}) placed at the drain side is termed as the second screen gate. As taken in our previous work [11], Tungsten disilicide (WSi_2) with work function 4.8 eV is taken as control gate along with $Hf_{0.27}Ta_{0.58}N_{0.15}$ with work function 4.6 eV as first screen gate and $Hf_{0.40}Ta_{0.46}N_{0.14}$ with work function 4.4eV as second screen gate. The x- and y-axes of the 2D structure are considered to be along the channel-upper oxide interface and the source-channel interface respectively.

The 2D channel potential $\varphi_k(x, y)$; $k = 1$, 2 and 3 in the channel region I, II and III can be obtained by solving the 2D Poisson's equation.

$$\frac{\partial^2\varphi_k(x,y)}{\partial x^2} + \frac{\partial^2\varphi_k(x,y)}{\partial y^2} = \frac{qN_a}{\varepsilon_{si}} \; ; \quad k = 1,2,3 \tag{1}$$

Following the method of parabolic potential approximation [12], the solution of Eq. (1) for regions I, II, and III corresponding to $k = 1$, 2, and 3 may be written as

$$\varphi_k(x, y) = a_{k0}(x) + a_{k1}(x)y + a_{k2}(x)y^2 \qquad k = 1,2,3 \tag{2}$$

where, a_{k0}, a_{k1} and a_{k2} are the arbitrary functions of x and could be derived by using the suitable boundary conditions as described in earlier work [11], as

$$a_{k0}(x) = \varphi_{sk}(x), \tag{3}$$

$$a_{k1}(x) = \frac{\varepsilon_{ox}\left[\varphi_{sk}(x) - V_{GS} + V_{fbk}\right]}{\varepsilon_{si}t_{ox}} \tag{4}$$

$$a_{k2}(x) = -\frac{\varepsilon_{ox}\left[\varphi_{sk}(x) - V_{GS} + V_{fbk}\right]}{\varepsilon_{si}t_{ox}t_{si}} \tag{5}$$

Note that, the characteristic length (λ) is an established tool to assess the SCEs TM-DG MOSFETs, as it indicates that how much drain electric field lines are penetrated into the channel region and hence controlled by drain region. Therefore, in order to get λ, we solve the Poisson's equation at the Si-SiO_2 interface ($y = 0$) as

$$\frac{\partial^2\varphi_{sk}(x)}{\partial x^2} - \frac{\varphi_{sk}(x)}{\lambda^2} = \beta_k \tag{6}$$

where, the characteristic length (λ) has been defined as

$$\frac{1}{\lambda^2} = \frac{2\varepsilon_{ox}}{t_{si}t_{ox}\varepsilon_{si}} \tag{7}$$

and

$$\beta_k = \frac{qN_a}{\varepsilon_{si}} - \frac{V_{GS} - V_{fbk}}{\lambda^2} \tag{8}$$

The general solution of Eq. (6) can be written as,

$$\varphi_{sk}(x) = A_k \exp(\eta x) + B_k \exp(-\eta x) - \frac{\beta_k}{\alpha} \tag{9}$$

where,

$$\eta = \frac{1}{\lambda} = \sqrt{\alpha} \tag{10}$$

Employing the boundary conditions as discussed in Ref. [10], coefficients A_k and B_k for region I, II and III can be written as

$$A_1 = \frac{V_{bi} + V_{DS} + \frac{\beta_3}{\alpha} - \left(V_{bi} + \frac{\beta_1}{\alpha}\right)\exp\left[-\eta\left(L_1 + L_2 + L_3\right)\right]}{2\sinh\left[\eta\left(L_1 + L_2 + L_3\right)\right]} + \\ + \frac{\frac{\left(\beta_1 - \beta_2\right)}{\alpha}\cosh\left[\eta\left(L_2 + L_3\right)\right] + \frac{\left(\beta_2 - \beta_3\right)}{\alpha}\cosh(\eta L_3)}{2\sinh\left[\eta\left(L_1 + L_2 + L_3\right)\right]} \tag{11}$$

$$B_1 = V_{bi} + \frac{\beta_1}{\alpha} - A_1 \tag{12}$$

$$A_2 = A_1 - \frac{(\beta_1 - \beta_2)}{2\alpha}\exp(-\eta L_1) \tag{13}$$

$$B_2 = V_{bi} + \frac{\beta_1}{\alpha} - A_1 - \frac{(\beta_1 - \beta_2)}{2\alpha}\exp(\eta L_1) \tag{14}$$

$$A_3 = A_1 - \frac{(\beta_1 - \beta_2)}{2\alpha}\exp(-\eta L_1) - \frac{\left(\beta_2 - \beta_3\right)}{2\alpha}\exp\left[-\eta\left(L_1 + L_2\right)\right] \tag{15}$$

$$B_3 = V_{bi} + \frac{\beta_1}{\alpha} - A_1 - \frac{(\beta_1 - \beta_2)}{2\alpha}\exp(\eta L_1) - \frac{\left(\beta_2 - \beta_3\right)}{2\alpha}\exp\left[\eta\left(L_1 + L_2\right)\right] \tag{16}$$

Hence, the final expression for channel potential can be written with the help of Eqs. (2), (9) and from Eqs. (11) to (16).

2.2 Threshold Voltage Modeling

As discussed earlier, the threshold voltage of the device will mainly be monitored by the control gate region of length L_1 with the highest work function φ_{m1}, since a conducting channel of the device will be established only if the control region is turned on. As the channel region is heavily doped ($\geq 10^{18}$ cm $^{-3}$), the conventional definition of threshold voltage can be

utilized. Therefore, the threshold voltage may be defined as the gate voltage at which the surface potential becomes twice of the Fermi potential, Φ_f. Hence,

$$\varphi_{s1\min} = 2\Phi_f \tag{17}$$

Further, the minimum value of potential $\varphi_{s1}(x)$ along channel can be obtained by solving $d\varphi_{s1}(x)/dx\big|_{x=x_{0\min}} = 0$ which in turn gives

$$x_{0\min} = \frac{1}{2\eta}\ln\left(\frac{B_1}{A_1}\right) \tag{18}$$

Now, on plugging Eq. (18) into Eq. (9), we obtain $\varphi_{s1\min}$ as

$$\varphi_{s1\min} = 2\sqrt{A_1 B_1} - \frac{\beta_1}{\alpha} \tag{19}$$

Thus, with the help of Eq. (17) and Eq. (19), the threshold voltage can be derived as

$$V_{th} = \frac{N \pm \sqrt{N^2 - 4(M - J)(r^2 + 1 - 2r)}}{2(r^2 + 1 - 2r)} \tag{20}$$

where,

$$r = \exp[-\eta l] + \sinh[\eta l] \tag{21}$$

$$N = 2m_1 r^2 + 2m_3 - 2yr - 2m_1 r - 2m_3 r + 2y - (2V_{bi} - 4\Phi_f)\sin^2 h(\eta l) \tag{22}$$

$$M = m_1{}^2 r^2 + m_3{}^2 - 2yrm_1 - 2m_1 m_3 r + 2m_3 y - m_1(2V_{bi} - 4\Phi_f)\sin^2 h(\eta l) \tag{23}$$

$$J = (V_{bi}{}^2 - 4\Phi_f^2)\sin^2 h(\eta l) - y^2 \tag{24}$$

The long channel threshold voltage, say V_{thL}, could be obtained from Eq. (20) as

$$V_{thL} = \underset{L\to\infty}{Lt}\, V_{th} = 2\Phi_f + V_{fb1} + \frac{qN_a\lambda^2}{\varepsilon_{Si}} \tag{25}$$

Where, V_{fb1} is the flat-band voltage in the region I and can be defined as,

$$V_{fb1} = \varphi_{m1} - \left[\chi_{si} + \frac{E_g}{2q} + V_t \ln\left(\frac{N_a}{n_i}\right)\right] \tag{26}$$

Hence, the threshold voltage roll-off could be found as

$$\Delta V_{th} = V_{thL} - V_{th} \tag{27}$$

3. RESULTS AND DISCUSSION

In this section, the analytical results of the surface potential and threshold voltage of the doped channel triple-material double-gate (DG) MOSFET,

calculated from our model, has been compared with the numerical simulation results obtained by the 2D device simulator ATLAS™ from SILVACO.[13] In addition to drift-diffusion (DD) and Fermi-Dirac statistics, field dependent mobility model has been employed. Modeling has been done under the assumption of Tungsten disilicide (WSi_2) with work function 4.8eV as control gate material along with $Hf_{0.27}Ta_{0.58}N_{0.15}$ with work function 4.6eV as first screen gate and $Hf_{0.40}Ta_{0.46}N_{0.14}$ with work function 4.4eV as second screen gate material. Figure 2 presents the surface potential variation against channel length for different V_{GS} and V_{DS}.

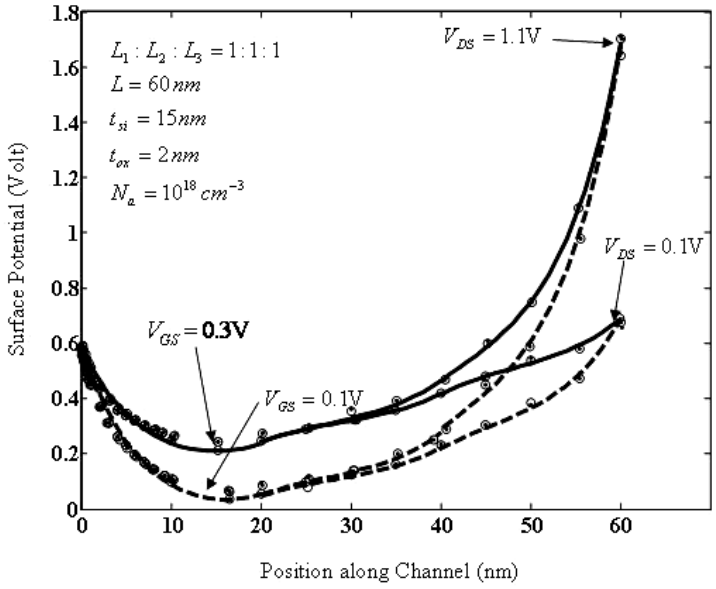

Fig. 2 *– Surface potential variation with channel length for different V_{GS} and V_{DS}*

The two steps occurred in the potential profile clearly indicate that the control gate near source region has least impact of drain variations which results in negligible DIBL. Figure 3 contains the variation of surface potential with channel length for different channel doping concentration,N_a. It is obvious from the figure that the barrier height can be raised by increasing the doping concentration in the channel region. The threshold voltage roll-off (ΔV_{th}) as a function of length of region I (L_1) for different channel thicknesses, t_{si}, is shown in Fig. 4. As expected, the threshold roll-off has been improved with decreasing silicon film thickness owing to better controllability of gate over channel region. Figure 5 shows the variation of threshold voltage as a function of length of region I (L_1) for different gate-oxide thickness, t_{ox}. It is clear from the figure that density of gate electric fields in the channel region reduces with thicker gate-oxide which, in turn, gives rise to threshold voltage roll-off. On the other hand, thinner gate-oxides furnishes better SCEs.

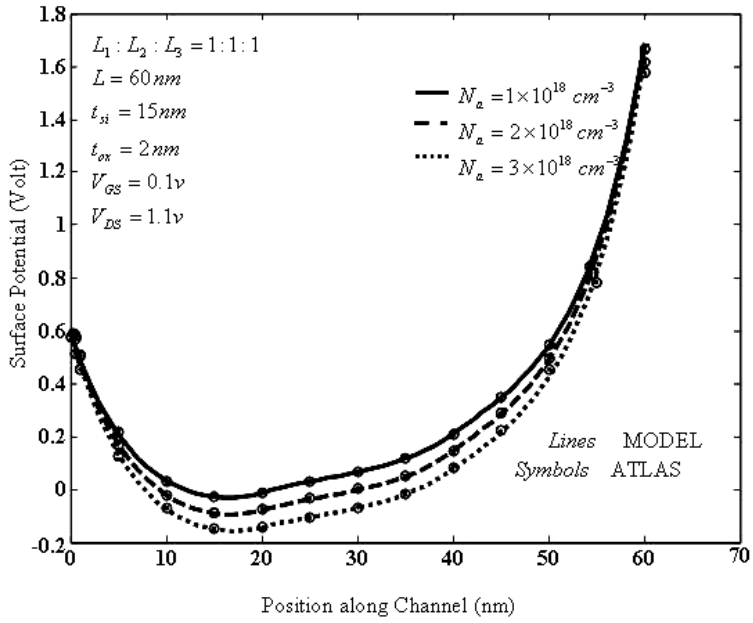

Fig. 3 *– Surface potential variation with channel length for different channel doping concentration* (N_a)

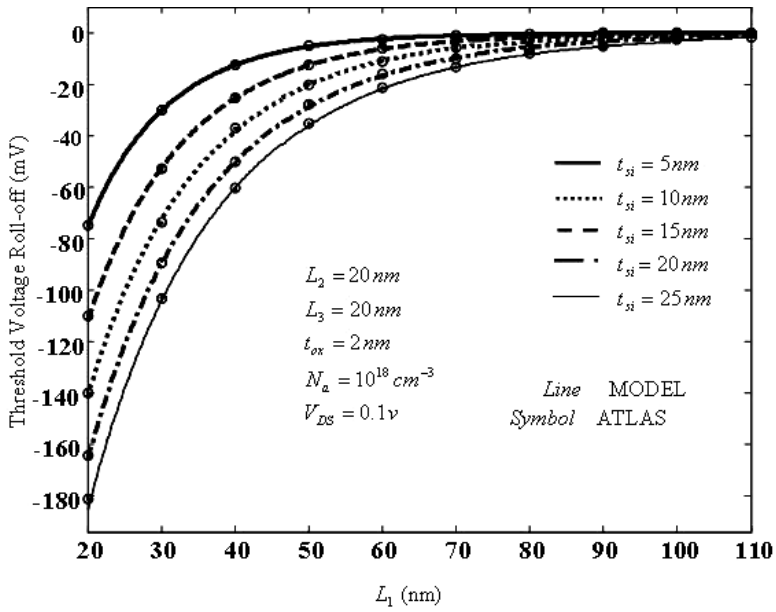

Fig. 4 *– Threshold voltage variation against* L_1 *for different channel thickness* (t_{si})

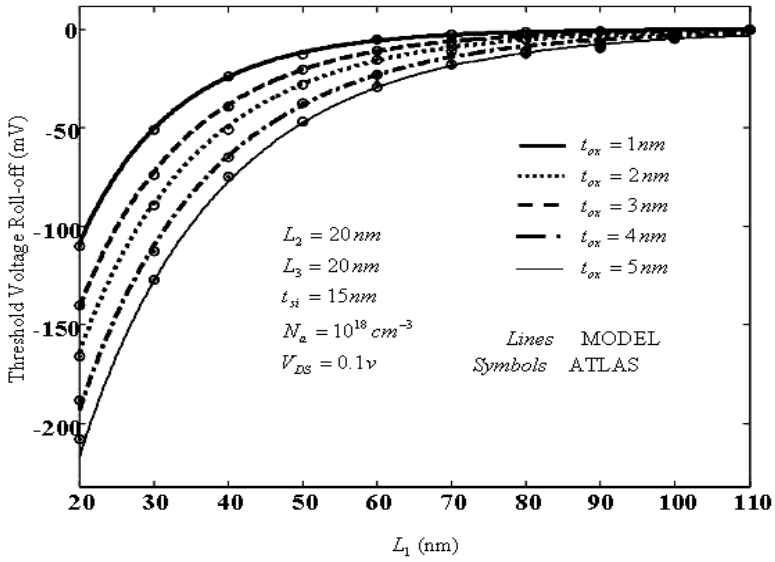

Fig. 5 *– Threshold voltage variation against* L_1 *for different oxide thickness* (t_{ox})

4. CONCLUSION

A two-dimensional short-channel threshold voltage model for doped channel triple-material double-gate (DG) MOSFET has been presented in this paper. Parabolic potential approximation method has been implemented to find the 2D potential distribution in the channel region. The doping dependency of surface potential has been found a good tool for increasing barrier height in the channel region. Besides this, the threshold voltage roll-off variations with gate oxide thickness and channel thickness are in good agreement with numerical simulation results extracted from ATLAS™, a 2D device simulator from SILVACO.

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