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EFFECT OF GRAIN SIZE ON THE THRESHOLD VOLTAGE FOR DOUBLE-GATE POLYCRYSTALINE SILICON MOSFET

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The effect of grain size (D) on the threshold voltage (V_{th}) for double gate polycrystalline silicon MOSFET is investigated theoretically in terms of grain boundary trap states (N_T). It is found that the threshold voltage (V_{th}) increases non-linearly with increasing silicon-oxide thickness (t_{ox}) for all values of grain size (D). However the threshold voltage is seen to have smaller values for same t_{ox} for the larger grains. This may be attributed to the reduction in the number of trap states in the depletion regions on either side of a grain boundary. Finally the dependence of threshold voltage (V_{th}) on various parameters such as the doping concentration, interface trap state density and field penetration from drain to source are explored out. The results of these findings are in good agreement with those available in the literature. For large grain poly silicon MOSFET the threshold voltage is seen to approach the single crystal value.

Keywords: *DOUBLE GATE POLY SILICON MOSFET, GRAIN SIZE AND THRESHOLD VOLTAGE.*

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1. INTRODUCTION

Poly-crystalline silicon Metal Oxide Semiconductor Field Effect Transistor has gained importance due to its advantages over the conventional MOSFET. Currently the poly Si devices are used in various fields such as solar cells, liquid crystal displays and integrated circuits because of their high electric field mobility and deriving current [1, 2]. Poly silicon Thin Film Transistors seem to be quite promising to be used in the fully integrated flat panel display system on panel (SOP) as a controller and memory circuits. However, these devices experience a high electric field near the drain region. This high electric field is the major cause of impact ionization in that region, which results in the accumulation of holes in the floating body device and hence produce a serious problem which is known as "kink effect" in the output characteristics [3]. Moreover, the performance of poly Si MOSFET is not good enough in terms of speed and current drive capability and large leakage current of poly Si MOSFET, which, leads to poor switching characteristics [4].

To reduce these undesired effects in Poly Si MOSFET, the multigate structured devices have been proposed, in a multigate MOSFET the operation is controlled at more than one gate on one hand and downscaling in CMOS-technology is done on the other hand thereby diminishing short channel effects [5, 6]. The most promising of such devices is the double gate

poly Si MOSFET which has shown a well proved performance improvement in terms of the reduced junction capacitance and junction isolation. As a result, the optimization of the channel length is possible which in turn becomes advantageous in carrier transport [7].

The threshold voltage is the most important device parameter for the design, modeling, simulations and utilization of Double Gate Poly Si MOSFET [8]. The threshold voltage in such a device is the minimum gate voltage at which the growth of inversion layer starts. It is common in the literature that the threshold voltage is defined as the gate voltage at which surface potential at the $Si - SiO_2$ interface becomes twice the Fermi potential of Semiconductor body. The threshold voltage for double gate poly silicon MOSFET is the key parameter in the understanding of the device speed and needs to be investigated. In this paper, we present an analytical expression for threshold voltage (V_{th}) by considering single energy trap level at grain boundary in channel of DG Poly Si MOSFET.

2. THEORY

In order to obtain an explicit expression for threshold voltage (V_{th}), a single trap energy level is assumed to exist at the grain boundary in Double Gate Poly Si MOSFET [9]. Writing the one dimensional Poisson equation as,

$$\frac{d^2\varphi}{dx^2} = \frac{-\rho(x)}{\varepsilon_{Si}} \tag{1}$$

Here ε_{Si} is the permittivity of poly Si. The total charge density $\rho(x)$ is substituted as [10],

$$\rho(x) = -q\left[2n_i \sinh\frac{q\varphi}{K_B T} + \frac{N_T}{D}\left\{f(E_t,(E_f + q\varphi)) - f(E_t, E_f)\right\}\right] \tag{2}$$

Where, E_t, E_f and f are the trap state energy level, intrinsic Fermi level and Fermi Dirac distribution factor of electrons for the trap states respectively. D is the average grain size and N_T trap states [11]. Thereby,

$$\frac{d^2\varphi}{dx^2} = -q\left[2n_i \sinh\frac{q\varphi}{K_B T} + \frac{N_T}{D}\left(f(E_t,(E_f + q\varphi) - f(E_t, E_f)\right)\right]\varepsilon_{Si}^{-1} \tag{3}$$

Integrating this equation with boundary condition, that $\varphi|_{at\ interface} \to \psi_S$ one obtains the total charge (Q_S) per unit area at the interface,

$$QS = -\varepsilon_{Si}\frac{d\psi_s}{dx} \tag{4}$$

or

$$Q_S = \pm\sqrt{2K_B T n_i \varepsilon_{si}}\left[4\sinh^2\left(\frac{q\psi_s}{2K_B T}\right) + \frac{N_T(E_T - E_f)}{K_B T n_i D}\right]^{1/2} \tag{5}$$

Now considering the total charge to be the sum of the trap charge (Q_T) at grain boundary and free charge (Q_f) in conduction band.

$$Q_S = Q_T + Q_f \tag{6}$$

Since the threshold voltage in DG Poly Si MOSFET is defined as the minimum gate voltage for which induced charge at interface are equal to the trapped charge at the grain boundary, we write,

$$\left|Q_S\right| = \left|qN_T\right| = Q_T \tag{7}$$

The applied gate voltage V_G in DG Poly Si MOSFET is partly dropped across the silicon oxide and partly across the semiconductor bulk material. Thus,

$$V_G = \frac{Q_T}{C_{ox}} + \psi_s + V_{FB} \tag{8}$$

Using equations (7) and (8), one can obtain,

$$V_G = \frac{\left|qN_T\right|}{C_{ox}} + \psi_S + V_{FB} \tag{9}$$

This is the equation for the threshold voltage [10] under the condition when the surface traps have been ignored. However, some traps present at semiconductor – silicon oxide interface, causes, a number of fabrication steps in VLSI and hole /electron injection [12, 13]. The distribution, density of surface states can be determined by using methods such as charge pumping and DCIV [14]. The electrons trapped at interface states develop a negative charge at the surface. This negative charge is equivalent to a voltage in opposition to the applied gate voltage, which, can be modeled by a threshold voltage shift toward higher value $V_G + \Delta V_{it}$. The term ΔV_{it} is the voltage corresponding to the interface traps [15]. When the value of drain voltage is larger than pinch off voltage, the drain depletion region moves closer to the source depletion region. This result in a significant field penetration from drain to source and the potential at the source is lowered, resulting in an increased injection of electrons over the reduced channel potential barrier. This penetration of the junction electric field into channel region causes barrier lowering which in turn leads to reduction in the threshold voltage [16]. This yield,

$$V_0 = \frac{\left|qN_T\right|}{C_{ox}} + \psi + V_{FB} + \Delta V_{it} - \frac{\sigma\varepsilon_{ox}\varepsilon_{si}}{\pi C_{ox} L^m} V_{ds} \tag{10}$$

Where σ and m are technology dependent fitting parameters, substituting the equation (5) in equation (10), the final expression for threshold voltage V_{th} is obtained as

$$V_{th} = \frac{\sqrt{2K_B T n_i \varepsilon_{Si}}\left[4\sinh\frac{q\psi_s}{2K_B T} + \frac{N_T(E_t - E_f)}{K_B T n_i D}\right]^{1/2}}{C_{ox}} + \tag{11}$$

$$+\psi_s + V_{FB} + \Delta V_{it} - \frac{\sigma\varepsilon_{ox}\varepsilon_{Si}}{\pi C_{ox} L^m} V_{ds}.$$

3. RESULTS AND DISCUSSIONS

The threshold voltage (V_{th}) for DG Poly Si MOSFET has been calculated in terms of different parameters and is ploted in figure1 for different value of average grain size (D). The parameters used in these calculation are $\sigma = 0.31$, $m = 2.67$, $\Delta V_{it} = 0.41$volts, $V_{FB} = -1.1$ volts, $T = 300$ K, $\varepsilon_{Si} = 11.9\ \varepsilon_o$, $\varepsilon_{ox} = 3.9\varepsilon_o$, $L = 1$ μm, $E_t = 0.661$ eV and $\psi_S = 2\ \varphi_f$, where φ_f is the Fermi potential. For the different values of D the threshold voltage is found to increase non-linearly with increasing silicon-oxide thickness (t_{ox}). An increase in threshold voltage is observed with the increasing t_{ox}. It may be due to reducing gate dielectric field. It is predicted that for large value of D the threshold voltage has smaller value for same t_{ox}. This may be attributed to the reduction in the trap states in depletion region on either side of a grain boundary.

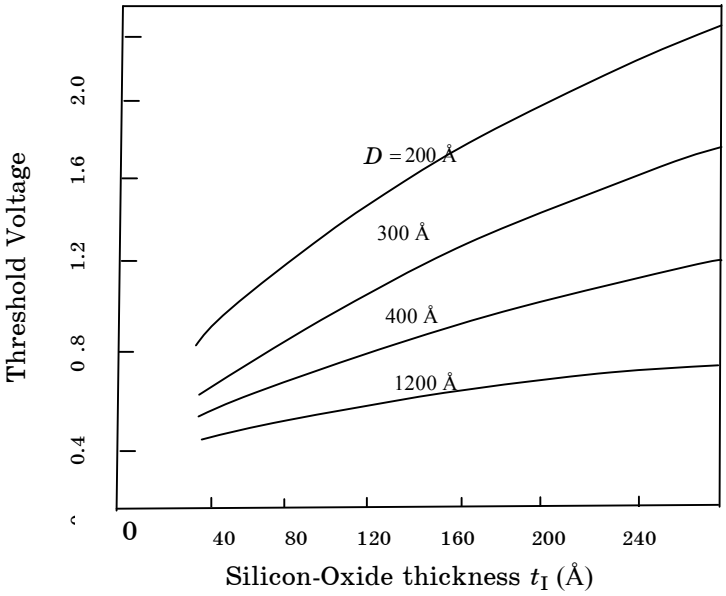

***Fig. 1** – Variation of threshold voltage (V_{th}) versus Silico – Oxide thickness tox for different grain size D when $V_{ds} = 0$ V*

Further investigations, shown in Figure 2, reveal that the threshold voltage increases non-linearly with doping concentration (N) for different values of grain size (D). On the basis of these calculations, the threshold voltage for Double Gate Poly Si MOSFET, with large grain size (D), is found to approach the single crystal value.

4. CONCLUSION

An analytical expression for threshold voltage (V_{th}) has been forwarded in terms of simple device parameters. The effect of grain size on the threshold voltage for DG Poly Si MOSFET has been explored. The formula is useful in explaining the effects of doping concentration, interface trap state density and field penetration from drain to source on the threshold voltage of the

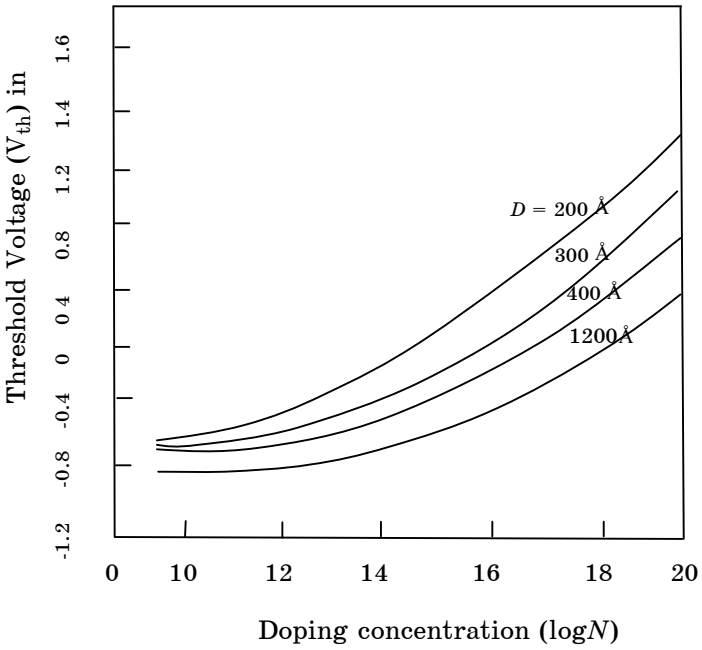

Fig. 2 *– Variation of threshold voltage (V_{th}) versus Doping concentration (N) for different grain size D when V_{ds} = 0 V*

device. It may finally forwarded that to have DG Poly Si MOSFET with larger values of threshold voltage, one must either increase the interface trap state density or apply a negative bias on back gate.

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