

Impact of SWCNT Band Gaps on the Performance of a Ballistic Carbon Nanotube Field Effect Transistors (CNTFETs)

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(Received 21 February 2017; published online 27 July 2017)

Band gap is an important property in designing single-walled carbon nanotube (SWCNT) for nanoelectronic devices. This paper describes the impact of SWCNT band gaps on the performance of a ballistic carbon nanotube field effect transistor (CNTFET) using the 2D numerical simulator. The results demonstrate that with the reduction in SWCNT band gap the performance parameters such as transconductance, output conductance, I_{on}/I_{off} current ratio, gain, and carrier injection velocity enhanced while the short channel effects subthreshold slope and drain-induced barrier lowering get suppressed. The enhanced device performance and reduced short channel effects of CNTFET with the reduction in SWCNT band gaps signifying that the CNTFET is a suitable nanoelectronic device for amplification purposes, low power analog and digital circuits, high-speed and low power applications.

Keywords: Band gap, SWCNT, CNTFET, Fettoy, Gate dielectric thickness.

DOI: [10.21272/jnep.9\(4\).04007](https://doi.org/10.21272/jnep.9(4).04007)

PACS numbers: 81.07.De, 85.35.Kt, 85.30.Tv

1. INTRODUCTION

Single walled (SW) and multi walled (MW) carbon nanotubes (CNTs) were fabricated in 1993 and 1991 respectively [1-2] while chirality controlled CNTs could not be fabricated in the past two decades because chirality was not controllable. But in the present scenario chirality based CNTs are possible to fabricate and characterize since Boris Yakobson et al. [3] has experimentally confirmed this in a theory that states “chirality of a nanotube controls the speed of its growth” while Jia Liu et al. [4] have successfully synthesized the (7, 6), (6, 5) and (7, 7) chirality based carbon nanotubes. Chirality dependent modeling of SWCNTs has been analytically described [5] while the chirality dependent properties of an armchair SWCNT has been demonstrated successfully [6]. Depending upon chirality (n, m), the tube is metallic or semiconducting. Wilder et al. [7] has shown that a SWCNT with $n - m = 3p$, where p is zero or any positive integer are metallic and all other tubes are semiconducting while Arora et al [8] has shown that a SWCNT is metallic if $(n - m) \bmod 3 = 1$ otherwise it is semiconducting. This can also be determined by the relation $n - m = 3p + q$ where p is an integer and the q is 0, 1 or 2. If q is zero, then the tube is metallic whereas if q is one, then SWCNT is semiconducting of mod 1 type and if q is 2, the SWCNT is semiconducting of mod 2 type.

The performance of a conventional silicon MOSFET has been enhanced as their channel length reduces but as soon as the channel length reaches 10 nm the short channel effect arises which degrades their performance. Therefore, it is very important for the researchers to search for alternative of silicon MOSFET devices [9-11]. Some novel nanoelectronic devices such as carbon-nanotube field effect transistor (FET), semiconductor-nanowire FET, and planar III-V compound semiconductor FET have been suggested to replace the silicon MOSFET to overcome those limitation challenges.

The carbon nanotube field effect transistors (CNTFETs) appears to be the most promising candidate for the next generation of integrated circuit devices and in order to explore the role of CNTFETs in future integrated circuits, it is necessary to evaluate their performance. However, to do that we require a model that can correctly explain the behavior of the CNTFETs so that the design and evaluation of circuits using these devices can be prepared [12-13]. In this work, the impact of SWCNT band gaps on the performance of a ballistic CNTFET have been studied using the nanohub simulation tool fettoy [14] based on the theory developed by A. Rahman [15].

2. BAND GAP OF SWCNT

The most important parameter in designing a SWCNT is chirality values that determine how the graphene sheet would be rolled up into a cylinder. The graphene sheet is rolled is represented by chirality (n, m). If $n = m = l$ where l is an integer then carbon nanotube formed is known as armchair SWCNT. If $n = l$ & $m = 0$, then carbon nanotube formed is known as zigzag SWCNT and if $n = 2l$ & $m = l$, then nanotube formed is known as chiral SWCNT. It means chirality (n, m) of the SWCNTs depends on the value of integer l e.g. when $l = 6$, we have (6, 6) armchair SWCNT, (6, 0) zigzag SWCNT and (12, 6) chiral SWCNT. The diameter of the SWCNT can be obtained as a function of n & m as [5]:

$$d_{(SWCNT)} \text{ (nm)} = 0.0783 \sqrt{n^2 + m^2 + nm} \quad (1)$$

and the band gap of the SWCNT can be obtained as a function of chirality values (n, m) as [16]:

$$E_g \text{ (eV)} = \frac{2\gamma_0 a_{c-c}}{d_{(SWCNT)}} = \frac{2\gamma_0 a_{c-c}}{0.0783 \sqrt{n^2 + m^2 + nm}} \quad (2)$$

where γ_0 (3 eV) and a_{c-c} (0.142 nm) are constant.

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This clearly shows that the diameter of the SWCNT depends on its chirality (n, m) and the bandgap of semiconducting tube is inversely proportional to its diameter. A comparison of the bandgap of semiconducting zigzag SWCNT for different chirality values is shown in Table 1. It has been observed that the simulated bandgaps obtained from the **CNTBands** [17] shows good agreement with the mathematical results. The bandgaps of (13, 0) & (19, 0) zigzag tubes fully matches but for other chirality values the band gap is half than the value found by Arora et al [8].

Table 1 – Comparison of bandgap of semiconducting SWCNT

SWCNT Chirality ($n = l, m = 0$)	Diameter $d_{SWCNT}(\text{nm})$	Band gap (E_g) in eV		
		Equ. (2)	Ref. [17]	Ref. [8]
(13, 0)	1	0.837	0.816	0.84
(19, 0)	1.5	0.572	0.563	0.58
(26, 0)	2	0.418	0.423	0.88
(32, 0)	2.5	0.340	0.343	0.70
(38, 0)	3	0.286	0.288	0.60

3. DEVICE DESCRIPTION

The structure of a ballistic CNTFET is shown in Fig. 1. In this structure, a semiconducting zigzag SWCNT has been used as channel material which is surrounded by an insulator layer which is finally surrounded by a metal contact known as gate terminal. The source and drain terminals are heavily doped. The gate voltage (V_G) induces the charge in the channel and to control the top of energy band between source and drain. The current flow from source to drain is made possible by lowering source-drain barrier and it can be calculated at the top of the barrier since the current is same throughout the channel.

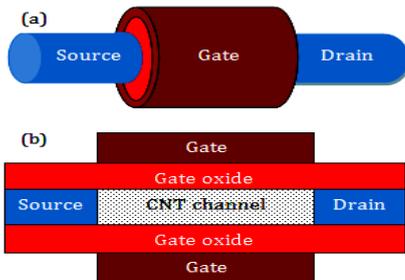


Fig. 1 – Structure of a ballistic CNTFET used by Fettoy (a) 3D view (b) 2D view

Two assumptions should be noted before the use Fettoy simulator: first, we assume that the metal-nanotube contact resistance is zero and second is that the carrier can transport through carbon nanotube without scattering (ballistic). The channel length is an important parameter in designing a CNTFET and in ballistic case, L (channel length) $\ll l$ (mean free path). Two types of scattering occurs in the channel either the diffusive or ballistic but the model used by **Fettoy** assumes ballistic conduction. Thus, there is no consideration of channel length as there would be no effect of length as long as ballistic conduction is maintained. **Fettoy** model focuses on the height of the energy barrier in the channel. The charge in the channel is con-

trolled by the height of the barrier. The input parameters used for various simulation results of CNTFET is shown in Table 2.

Table 2 – Input parameters used for various simulation results of CNTFET

Input Parameters	Value of Parameters	
	Default value	Range
Nanotube diameter	1 nm	0 nm to 1000 nm
Gate insulator thickness	1.5 nm	0 nm to 1000 nm
Gate Insulator dielectric constant	3.9 (SiO ₂)	0 to 50
Ambient Temperature	300 K	50 K to 1000 K
Initial gate voltage	0 (V)	- 5 V to 5 V
Final gate voltage	1V	- 5 V to 5 V
Gate voltage bias points	13	0 to 60
Initial drain voltage	0 V	- 5 V to 5 V
Final drain voltage	1 V	- 5 V to 5 V
Drain voltage bias points	13	0 to 60
Threshold voltage	0.32 V	- 5 V to 5 V
Gate control parameter	88	0 to 1
Drain control parameter	0.035	0 to 1
Series resistance	0 $\Omega\text{-}\mu\text{m}$	0 or greater than 0

4. ANALYTICAL MODEL

The two-dimensional (2D) model for ballistic CNTFET as shown in Figure 2 is based on the model planned by A. Rahman et al. [15] which has been an extension of the earlier work done by K. Natori [18]. The model of ballistic CNTFET consists of three capacitors, which represents the consequence of the three terminals on the potential at the top of the barrier and the shaded region indicates the mobile charge which is determined by the local density of states at the top of the barrier, location of the source and drain Fermi levels (E_{F1} & E_{F2}) as well as self-consistent potential at the top of the barrier (U_{scf}).

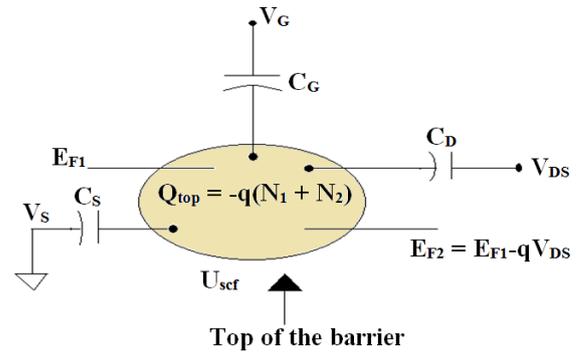


Fig. 2 – 2D model for a ballistic CNTFET

When the incurable biases are nil, the equilibrium electron density at the top of the barrier is

$$N_0 = \int_{-\infty}^{+\infty} D(E) f(E - E_F) dE \quad (3)$$

where $D(E)$ is local density of states at the top of the barrier and $f(E - E_F)$ is the equilibrium Fermi function. $D(E)$ is zilch for negative values of its argument which represents the minimum of the density of states and is specified as $E = 0$ in equilibrium. The source terminal is always grounded in this model but applying a bias to the gate and drain terminals causes the self-consistent potential at the top of the barrier to become U_{scf} and populates the states at the top of the barrier by two different Fermi levels. The positive velocity states are populated by the source and the negative velocity states are populated by the drain, as described by

$$\begin{aligned} N_1 &= \int_{-\infty}^{+\infty} D(E - U_{scf}) f(E - E_{F1}) dE \\ N_2 &= \frac{1}{2} \int_{-\infty}^{+\infty} D(E - U_{scf}) f(E - E_{F2}) dE \end{aligned} \quad (4)$$

where $E_{F1} = E_F$ and $E_{F2} = E_F - qV_{DS}$. It is convenient to simplify equation (4) by defining

$$\begin{aligned} f_1(E) &\equiv f(E + U_{scf} \mp E_{F1}) \\ f_2(E) &\equiv f(E + U_{scf} \mp E_{F2}) \end{aligned} \quad (5)$$

and substituting them back into equation (4) to produce the final equations

$$\begin{aligned} N_1 &= \frac{1}{2} \int_{-\infty}^{+\infty} D(E) f_1(E) dE \\ N_2 &= \frac{1}{2} \int_{-\infty}^{+\infty} D(E) f_2(E) dE \end{aligned} \quad (6)$$

With equation (6), the total electron density at the top of the barrier is $N = N_1 + N_2$ and can be determined if the arbitrary density of states $D(E)$, the source and drain Fermi levels and the self-consistent potential U_{scf} are known. All parameters are given except U_{scf} and the method for determining the U_{scf} is presented below.

The self-consistent potential is determined by solving the two-dimensional Poisson equation as represented by the 2D replica in Figure 2 with the common terminal evaluated at the bias induced charge, $N = (N_1 + N_2) - N_0$. Ignoring mobile charge in the channel, the Laplace potential at the top of the barrier is then

$$U_L = \mp q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) \quad (7)$$

The three α 's describe how the gate, drain and source control the Laplace solution and are given by

$$\alpha_G = \frac{C_G}{C_T}, \quad \alpha_D = \frac{C_D}{C_T}, \quad \alpha_S = \frac{C_S}{C_T} \quad (8)$$

where C_T is the parallel combination of three capacitors C_G , C_D , C_S . For an optimally constructed MOSFET, the gate controls the potential in the channel which means that $\alpha_G \approx 1$, α_S , $\alpha_D \approx 0$. The mobile charge potential is then calculated as

$$U_P = \frac{q^2}{C_T} \Delta N \quad (9)$$

When a positive bias is applied to the drain and gate terminals, the potential energy at the top of the barrier is pressed down according to U_L , but the charge causes the potential to float up according to U_P . The entire self-consistent potential U_{scf} is the superposition of these two potentials

$$\begin{aligned} U_{scf} &= U_L + U_P = \\ &= -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) + \frac{q^2}{C_T} \Delta N \end{aligned} \quad (10)$$

where the charging energy, $UC = q^2 / C_T$

With equations (4) and (10), the united nonlinear equations for N and U_{scf} can be iteratively solved to find the carrier density and the self-consistent potential at the top of barrier.

Taking $J(E)$ as the "current-density-of-states", the drain current is determined by

$$\begin{aligned} I_D &= \int_{-\infty}^{+\infty} J(E) [f_1(E) - f_2(E)] dE \\ I_D &= \frac{2qk_B T}{\pi \hbar} \int_{-\infty}^{+\infty} [f(E - E_{F1} - U_{scf}) f(E - E_{F2} - U_{scf})] dE \end{aligned} \quad (11)$$

5. RESULTS AND DISCUSSION

In this section, the performance parameters of ballistic CNTFET such as drive current (I_{on}), I_{on}/I_{off} current ratio, transconductance (g_m), output conductance (g_d), gain (A_v), carrier injection velocity (v_{inj}), sub-threshold slope (SS) and drain induced barrier lowering (DIBL) have been described as the band gap of SWCNT changed which depends on chirality and diameter while all other parameters are kept fixed but the number of bias points (N) chosen here are 11.

5.1 Drive Current (I_{on}) and I_{on}/I_{off} Current Ratio

Drive current (I_{on}) is the value of drain-source current (I_{DS}) at $V_{GS} = V_{DS} = V_{DD} = 1$ V and leakage current (I_{off}) is the drain-source current (I_{DS}) at $V_{GS} = 0$ V & $V_{DS} = V_{DD} = 1$ V. Fig. 3 displays the impact of band gaps on drive current (I_{on}) and I_{on}/I_{off} current ratio of CNT-FET. It can be seen that the drive current (I_{on}) increases with decrease in band gap of the SWCNT and maximum drive current is achieved at higher chirality (38, 0) with lower band gap due to the maximum number of subbands of this chirality as well as the requirement of low energy for the transfer of electrons from valence to conduction band. No effect of band gap shows on the leakage current since it remains constant. The figure further divulges that the I_{on}/I_{off} current ratio increases with the decrease in band gap due to the increase in I_{on} and constant leakage current (I_{off}), therefore, device switches fast from off-state to on-state.

5.2 Transconductance (g_m) and Output Conductance (g_d)

Transconductance (g_m) is an important property that determines the performance of any FET and defined as the ratio of change in drain-source

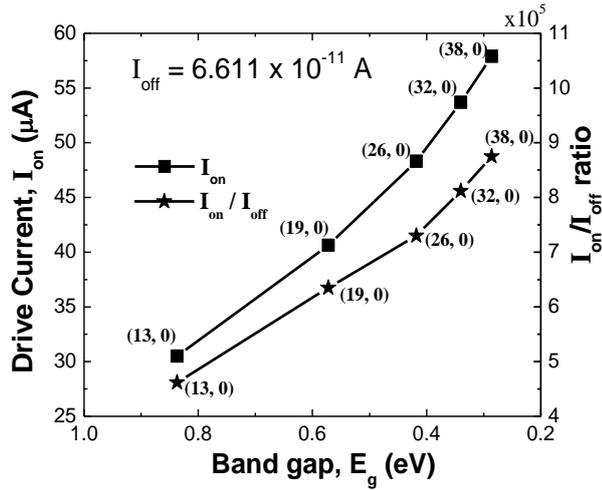


Fig. 3 – Drive current (I_{on}) and I_{on}/I_{off} ratio of CNTFET

current (I_{DS}) to the change in gate-source voltage (V_{GS}) at constant drain-source voltage (V_{DS}). This property determines the controllability of gate on the channel. It has been observed in Fig. 4 that the transconductance of the device increases with the decrease in band gap which indicate the stronger control of gate on the channel. The SWCNT with minimum chirality value (13, 0) having maximum band gap shows lower transconductance and SWCNT with maximum chirality value (38, 0) having minimum band gap shows higher transconductance. This figure further shows the significant enhancement in output conductance occurs with the reduction of band gap of SWCNT channel.

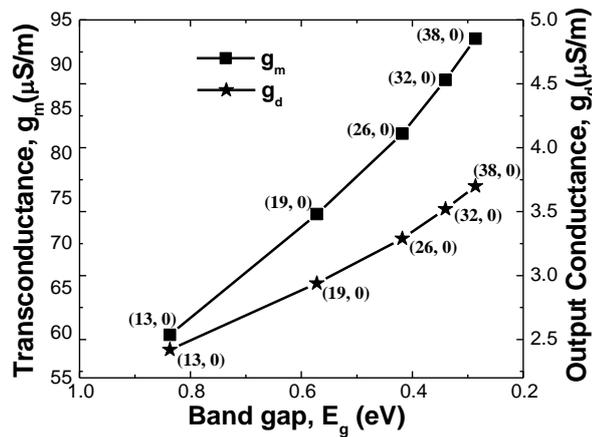


Fig. 4 – Transconductance (g_m) and output conductance (g_d) of CNTFET

5.3 Gain (A_v) and Carrier Injection Velocity (v_{inj})

Gain of the device is defined as the ratio of transconductance to the output conductance. In order to use the device for amplification, a high gain is required. Fig. 5 illustrates the effect of band gap on the gain which can be clearly seen that the gain of the device is increased with the decreased in band gap indicating

that the CNTFET can be used as an amplification purposes. This figure also shows the effect of band gap on carrier injection velocity. As we know there is a direct relationship of carrier injection velocity with drain current and drain current with band gap so as the band gap is decreased the carrier injection velocity is increased. Maximum chirality values of SWCNT having lower band gap achieved high gain and high carrier injection velocity of CNTFET.

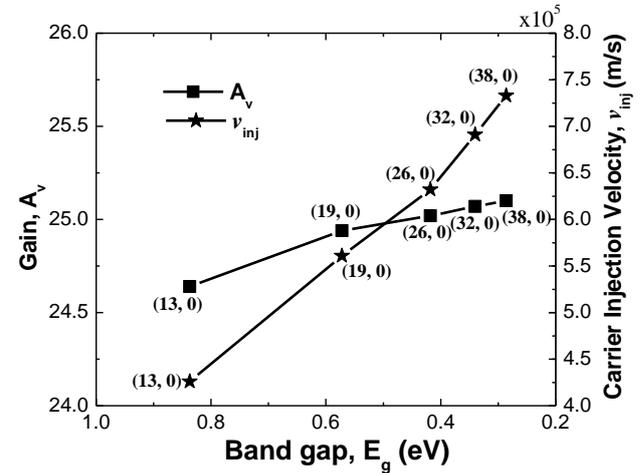


Fig. 5 – Gain (A_v) and carrier injection velocity (v_{inj})

5.4 Short-channel Effects

The short-channel effects are attributed to two physical phenomena such as (i) The limitation imposed on electron drift characteristics in the channel and (ii) The modification of the threshold voltage due to the shortening of channel length [28]. Two short channel effects have been discussed such as subthreshold slope (SS) and drain induced barrier lowering (DIBL). The drain current increases exponentially below V_{th} when plotted in logarithmic scale and the subthreshold slope is the number of millivolts of increase in gate voltage needed to increase the drain current by a factor of 10. This property is very important for low power applications.

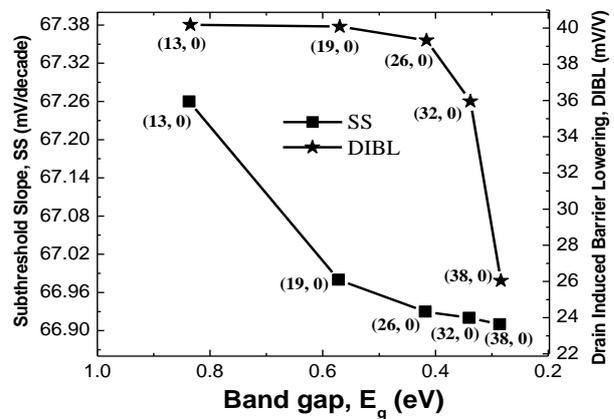


Fig. 6 – Subthreshold slope (SS) and drain induced barrier lowering (DIBL)

When the I_{DS} - V_{GS} curve of a device is steeper, the subthreshold slope will improve. For well designed

MOSFET, SS is less than 80 mV/decade and his lowest theoretical limit for SS is 60 mV/decade at room temperature. It has been observed in Fig. 6 that the SS is 67.26 mV/decade for chirality value (13, 0) having band gap of 0.837 eV and reduces with the decrease in band gap values. This is attributed to superior control of the gate over the channel. When the barrier height for channel carriers at the edge of the source goes down, DIBL effect occurs because of the influence of the drain electric field. For a well designed MOSFET, DIBL is less than 100 mV/V. It can be seen from the fig. 6 that the DIBL is 40.19 mV/V for chirality (13, 0) having band gap of 0.837 eV and it reduces with the further decrease in band gap of SWCNT. Maximum improved values of SS and DIBL occurs for chirality values (38, 0) having minimum band gap.

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6. CONCLUSION

In this paper, the impact of SWCNT band gaps on the performance of CNTFETs has been reported. It has been concluded that the reduction in band gaps of SWCNT causes an increase in I_{on}/I_{off} current ratio which leads to a high drive current (I_{on}). Other performance parameters such as transconductance, output conductance, gain, and carrier injection velocity of CNTFETs have been enhanced with the decrease in SWCNT band gaps. The short channel effects such as subthreshold slope and drain induced barrier lowering also improve which are very close to its theoretical limit. Thus, the band gap of SWCNT channeled controls the performance and short channel effects of CNTFETs meaning that it replace the conventional silicon MOEFET in future CMOS technology.