MODELING OF THRESHOLD VOLTAGE AND DRAIN CURRENT OF UNIAXIAL STRAINED p-MOSFETs

Amit Chaudhry[1]*, Sonu Sangwan*[2]*, Jatindra Nath Roy*[3]

[1] UIET, Panjab University, Sector − 25, 91160014, Chandigarh, India
  E-mail: amit_chaudhry01@yahoo.com

[2] UIET, Panjab University, Sector − 25, 91160014, Chandigarh, India

[3] Solar Semiconductor Private Limited, Hyderabad, India

An analytical model describing the threshold voltage and drain current in strained-Si p-MOSFETs as a function of applied uniaxial strain applied at the gate has been developed in this paper. The uniaxial stress has been applied through the silicon nitride cap layer. The results show that the threshold voltage falls and drain current rises due to applied uniaxial strain. The results have also been compared with the experimentally reported results and show good agreement.

Keywords: MOBILITY, STRAINED−Si, MODEL, NUMERICAL.

1. INTRODUCTION

The reduction in carrier mobility is a major cause of drain current degradation in scaled down MOSFETs due to the high vertical electrical fields in the silicon substrate. This reduces the speed of the device. To control this effect, strained silicon technology has evolved in the past few years as a replacement to silicon in substrate. Various models/experiments have been developed in the past several years for the drain current and threshold voltage estimation of the stressed silicon MOSFETs. Xu.Q et al [1],Belford et al [2], Wei Zhao, et al [3], Wacker et al [4] have studied the drain current under uniaxial stress experimentally. Bufler et al [5] have numerically modeled the threshold voltage and drain current under the uniaxial stress conditions. There is very little work done in this area at present in the area of development of analytical models to the best of the knowledge of the authors.

It would be appropriate to say here that there is a strong requirement of an analytical model which is simple and can be easily embedded into SPICE and largely accurate. An attempt has been made in this paper to semi analytically model the threshold voltage and drain current under the condition of applied uniaxial strain at the metal gate.
The paper is organized as follows. Section II deals with the modeling of threshold voltage and drain current of biaxial strained silicon MOSFET. Section III details the results and discussions. Conclusion is given in section IV.

2. MODELING

Fig. 1 is shown below which is used for all modeling purposes in this paper.
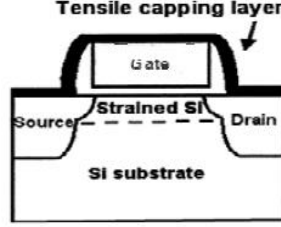
Fig. 1 − *Cross-sectional view of uniaxially strained-bulk-si MOSFET*

2.1 Threshold voltage modeling

The threshold voltage is modeled by evaluating the flatband voltage, depletion charge and the surface potential in the presence of uniaxial stress. The depletion charge density is given by solving Poisson equation in the substrate in depletion region.

$$Q_{depl} = \left(2e_0 e_{si} q N_a \varphi_{ss}\right)^{1/2} \tag{1}$$

V_{ts} is a strained threshold voltage given by

$$V_{ts} = -V_{fbs} - (Q_{depl} / C_{ox}) - \varphi_{ss} \tag{2}$$

The flat band voltage V_{fbs} is given by

$$V_{fbs} = -\left\{\varphi_m - (\chi_s + \Delta E_g + E_g - q\varphi_{fs})\right\} + Q_o / C_{ox} \tag{3}$$

χ_s is the electron affinity increase at the silicon substrate side and is increased due to decrease in energy gap, φ_{ss} is the surface potential in weak inversion = $2\varphi_{fs}$, φ_{fs} is $V_t \ln(N_a / n_{is})$, $V_t = kT/q$, $n_{is} = n_i \exp(\Delta E_g / 2kT)$. E_g is unstrained silicon bandgap, ΔE_g decrease in energy gap due to strain, N_a is the substrate doping, t_{ox} is the oxide thickness, Q_o is the interface charge density. For values, refer Table 1 at the end of the paper.

2.2 Drain current modeling

The drain current is obtained by SPICE level 1 model by the parameters applicable for uniaxial strain i.e. threshold voltage and the hole mobility. The equations 4a − 4c are given below:

$$I_{ds} = 0 \text{ for } V_{gs} > V_{ts} \tag{4a}$$

$$I_{ds} = k_n \left\{2(V_{gs} - V_{ts})V_{ds} - V_{ds}^2\right\} \text{ for } V_{ds} > V_{gs} - V_{ts} \tag{4b}$$

$$I_{ds} = k_n (V_{gs} - V_{ts})^2 \text{ for } V_{ds} \leq Vgs - V_{ts} \tag{4c}$$

$k_n = \mu_s \, C_{ox} W \, / \, 2L$, I_{ds} is the drain current (μA), Width of the transistor W (µm) and Length of the transistor is L (µm). C_{ox} is the gate oxide capacitance (Fm^{-2}) = $\varepsilon_o \varepsilon_{si} \, / \, t_{ox}$, V_{ds} is negative, μ_s is the hole mobility under uniaxial strain conditions as given by [6].

3. RESULTS AND DISCUSSIONS

Firstly, we have modeled the threshold voltage for the strained silicon MOSFET for various device parameters as given in Table 1. The Figure 2 shows a variation of threshold voltage with the substrate concentration and applied strain as the third parameter. The threshold voltage falls clearly when the strain is applied. This is due to the decrease in the energy gap and less voltage is required to obtain inversion at the metal gate. Figure 3 shows the threshold voltage variation for uniaxial strained p-MOSFET and compared well with the experimental reported results [4]. Figure 4 shows the drain current variation in the increase strained and unstrained conditions. The

**Table 1** − *Silicon MOSFET parameters used in simulation*

Parameter	Value
Applied Strain	$0 - 0.124$
Source/Drain and poly silicon doping	2×10^{20} cm^{-3}
Gate oxide thickness	22 nm
Work function of gate material	4.2 eV
Width	20 micron
Length	20 micron
Q_o	8×10^{-5} Ccm^{-2}.
E_g	1.12 eV
ΔE_g	-0.619ε [6]
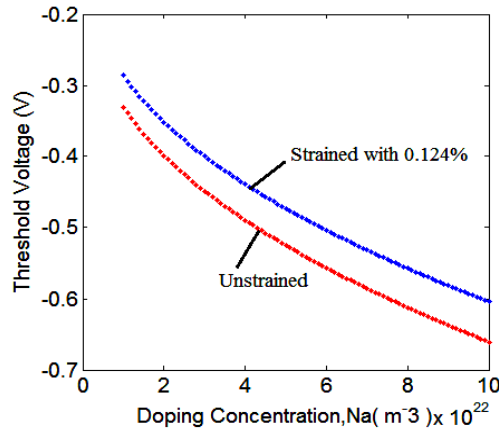
Fig. 2 − *Variation of threshold voltage of strained and unstrained-*Si $p-$ *MOSFETs with doping concentration (*Na*). The parameters are oxide thickness (t_{ox}) = 8 nm, Strain = 0.124 %*
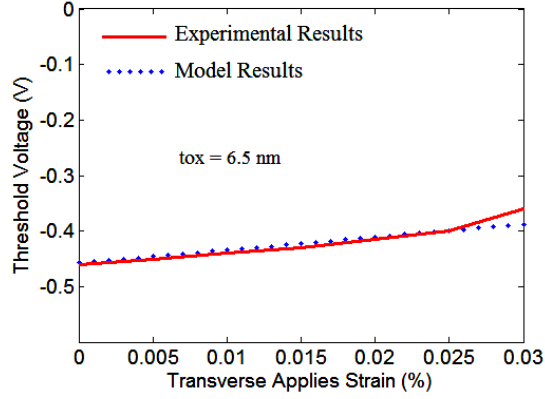
Fig. 3 − *Variation of threshold voltage of uniaxial strained-Si p − MOSFETs with applied strain at room temperature is shown. Reported experimental results [4] are shown by the red line. Data calculated with the model developed in this paper are shown by the blue symbols*
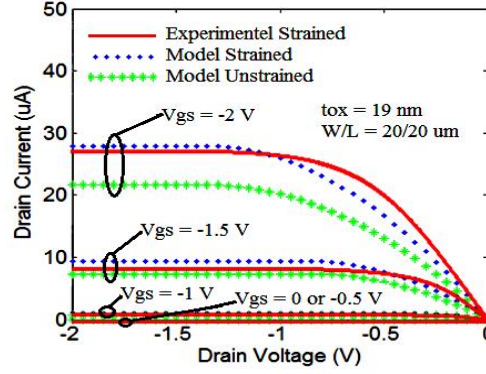
Fig. 4 − *Variation of drain current (I_{ds}) with the drain-source voltage (V_{ds}) at different values of gate-source voltage (V_{gs}) for p − MOSFETs at room temperature is shown. Reported results [3] with 0.124 % strain are shown by the red lines. Data calculated by the model developed in this paper with 0.124 % strain are shown by the blue symbols. The unstrained results are shown by the green symbols*

figure shows an increase of drain current due to strain. This is because strain increases the hole mobility and reduces the threshold voltage. Thus the drain current increases. The results match closely with the experimental results [3].

4. CONCLUSIONS

The analytical model developed in this paper shows a decrease in threshold voltage and increase of drain current under uniaxial strain conditions. The results match closely with the reported results proving the validity of the model.

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