ELECTROSTATICS OF SILICON NANO TRANSISTOR

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Nano Transistor represents a unique system for exploring physical phenomena pertaining to charge transport at the nano scale and is expected to play a critical role in future evolution of electronic and optoelectronic devices. This paper summarizes some of the essential electrostatics of nano Metal Oxide Semiconductor Field effect Transistor (MOSFET) and their electrical properties. Though the general focus of this work is on surface potential yet the first part presents a brief discussion of the independence of charge at the top of the barrier in the channel of MOS Transistor on Drain voltage. The quantum capacitance is discussed at length. The superposition theorem is used, thereafter, to obtain an expression for self consistent potential in the channel. Finally the I-V characteristics of the device are explored using Landauer formalism. The simulated results for a device are observed to represent the realistic behaviour of the device.

1. INTRODUCTION

A substantial progress in Integrated circuit technology is primarily due to downscaling trends of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) that have continued even to the present day [1, 2]. Recently, various semiconductor nanowire (NW) devices have drawn considerable attention because of their possible applications in future electronics and optoelectronics. Continued MOSFET scaling has led to the study of non planer FET geometries that can provide better short-channel control than conventional planer FETs [3-6]. In particular, gate-all-around (GAA) or surround-gate (SG) FETs with thin nanowire channel can provide superior electrostatic characteristics that will allow continued scaling beyond what is possible with planer technology [3, 15]. Quantum confinement effects make modelling of nanowire (NW) transistors a complex problem [12, 14]. While there are many studies in the literature on the modelling of nanowire transistors based on Non Equilibrium Greens' Function or Monte Carlo approach [5, 16]. The physics related to the operation of nanowire transistors need to be well articulated. Ballistic Transport and realistic sub band parameters can be developed for circuit design using simulation programme with integrated circuit emphasis like simulations. Among the different materials considered for growing nano material (nanowire), Si has been studied extensively due to its compatibility with conventional Si CMOS technology [13].

2. THEORY

Natori proposed the model for MOSFET in the ballistic regime [7]. In his model, there are two important simplifications that were made. 1. We neglected 2-D electrostatics, which is important in short-channel MOSFETs. 2. We assumed that above threshold the charge at the top of the barrier is approximately independent of drain bias. Now we will discuss these two issues here separately [9].

2.1 Role of Quantum Capacitance

The MOS electrostatics is most important thing to understand about the MOSFET. Fig. 1(a) shows the energy diagram. We see that the positive voltage at the gate, which lower the charge carrier's energy and bends the band down by an amount $q\psi_s$, appears partially across the oxide layer and partly across the depletion region of the semiconductor [10].

$$V_G^{'} = \psi_S + V_{ox} \, ,$$

where $V_G^{'} = V_G - V_{FB}$ and V_{FB} is flat band Voltage. The voltage across the oxide is obviously related to the charge on either side, divided by capacitance. Hence,

$$V_{OX} = \frac{-Qt_{ox}}{\varepsilon_{ox}} = \frac{-Q_x\left(\psi_s\right)}{C_{OX}} \, ,$$

where permittivity of the oxide (SiO_2) and C_{OX} is the oxide layer capacitance per unit area. Hence equation (1) may be written as,

$$V_G^{'} = \frac{q_{ns}}{C_{OX}} - \frac{E_i(o)}{q}$$

$$E_i(o) = -qV_G^{'} + \frac{q^2 n_s}{C_{ox}}$$

(1)

Here, q is the energy of charge carrier at the top of the barrier. That gives us the information about Self Consistent Potential (U_{SLF}). We will solve the expression for it in next section. Here, we will solve modified one-dimensional (1-D) Poisson equation for the surface potential [14].

$$\frac{d^2\psi_s}{dy^2} - \left(\frac{\psi_S\left(y\right) - V_{GS} - V_{bi}}{\lambda^2}\right) = -e\frac{\rho\left(y\right)}{\varepsilon_{si}}$$

Here, $V_{bi} = \frac{K_B T}{q}\ln\left(\frac{N_A N_D}{n^2{}_i}\right)$ is built in potential of p-n junctions between the Source/Drain and channel under flat band condition while at threshold it becomes $V_{bi} = \frac{K_B T}{q}\ln\left(\frac{N_D}{N_A}\right)$: The geometrical scaling length $\lambda = \sqrt{\frac{\varepsilon_{si} t_{si} t_{ox}}{\varepsilon_{ox}}}$
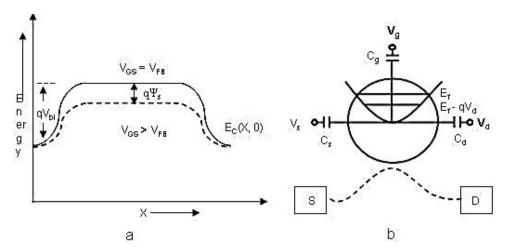
Fig. 1 − *Conduction band energy vs. position in the bulk silicon at equilibrium (a) and Capacitor model for 2-D electrostatic (b)*

provides a measure how effectively the gate potential (V_G), modulate the surface potential ψ_s. Semiconductor capacitance [9], (above threshold)

$$C_s^{\cdot} = -\frac{dQ_s}{d\psi_s} = -\frac{dQ_i}{d\psi_s} = C_{inv}.$$

This is closely related to quantum capacitance and become important as device enters into nanoscale (thickness of oxide layer tending towards zero). Under such circumstances the above expression for quantum capacitance reduces to [9],

$$C_s^{\cdot} = -\frac{qdn_s}{d\psi_s}$$

$$C_s^{\cdot} = q\int_0^\infty N_{2D}\frac{\partial f}{\partial \psi_s}dE = q^2\langle N_{2D}\left(E_f\right)\rangle \tag{2}$$

where the 2-D density of state $N_{2D} = {m_{Di}s}/{\pi\hbar^2}$ and m_{Di} is the density of state effective mass. This reveals that the quantum capacitance depends on the average 2-D density of state at Fermi level. The charge at the top of the barrier is also related to the potential to the potential at the top of the barrier [9].

$$n = n^+ + n^- \tag{3}$$

$$n = \frac{N_{2D}}{2}F_o\left(\eta_F\right) + \frac{N_{2D}}{2}F_o\left(\eta_F - qV_D\right) \tag{4}$$

According to this model, change in gate potential produces a change in surface potential. And this can be written as,

$$\delta E_1 = -\frac{q\delta V_G}{1 + C_S/C_{OX}} \tag{5}$$

Here C_s is quantum capacitance or surface capacitance.

2.2 2-D Electrostatics

In this section we will examine the self-consistent potential by considering a MOSFET is regarded as a three capacitor as shown in fig. 1(b), which is generally evaluated by the external voltage and charge in the channel. Hence by superposition theorem, the self-consistent potential, is $U_{SLF} = U_L + U_P$, where first term is the solution of Laplace equation by assuming that there is no charge carrier is present in the channel and second is the solution of Poisson equation in the presence of charge in the channel. Solution of Laplace equation is,

$$U_L = -q\left(\alpha_G V_G + \alpha_D V_D + \alpha_S V_{SG}\right)$$

where $\alpha_G = C_G/C_\Sigma$, $\alpha_D = C_D/C_\Sigma$, $\alpha_S = C_S/C_\Sigma$, C_D, C_G and C_S refer to the three capacitors that describe the electrostatics control of the three electrodes. Solution of Poisson equation is, $U_P = q^2 n_s/C_\Sigma$, Hence complete potential will be,

$$U_{SLF} = -q\left(\alpha_G V_G + \alpha_D V_D + \alpha_S V_{SG}\right) + \frac{q^2 n_s}{C_\Sigma}$$

3. ELECTRONIC TRANSPORT

For the calculation of drain current through the nano MOS Transistor we employ the Landauer formalism. This is widely used to evaluate the current in a situation for which quantum mechanical tunneling dominates. That is drain current is,

$$I = \left(I_{L \to R} - I_{R \to L}\right)$$

$$I = -\frac{2q}{h} \sum \int [T_n(E)f_L(E - E_{FL}) - T'_n(E)f_R(E - E_{FR})]dE \tag{6}$$

For elastic scattering $T(E) = T(E_F)$,

And for the approximation $f_L\left(E - E_{FL}\right) - f_R\left(E - E_{FR}\right) \approx -\frac{\partial f}{\partial E}\left(qV_D\right)$ the final result for current is,

$$I = -\frac{2q^2}{h} \sum_{n=1}^{M} T_n(E_F)V_D \tag{7}$$

where M_V = no. Of transverse modes and $T(E_F)$ is average transmission coefficient at Fermi energy.
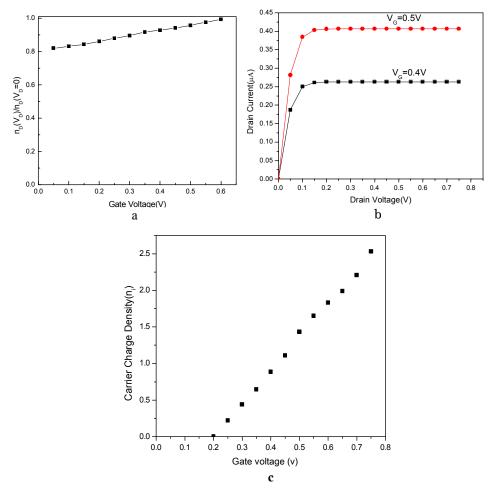
Fig. 2 *– Relative charge density, N_D $(V_D)/N_D$ $(V_D = 0)$ versus Drain voltage (a), Drain voltage versus drain current (b), Carrier charge density versus gate voltage (c)*

4. RESULTS & DISCUSSIONS

A number of modelling and simulation has been carried out on the D-G MOSFET geometry using 10 nm. Source-Drain extension (channel length) and different gate lengths with 1.5 nm silicon die oxide layers [8]. A hierarchy of models with increasing interest in this field is to be present some Analytical results that illustrate the capability of the work. The present model is an idealised structure. For calculation, the length of the source, channel and drain regions are all equal. The gate material is ideal n^+ polysilicon whose work function is equal to the conduction band edge. The drain and the source region are uniformly doped and the channel region is intrinsic having length 10nm. The oxide thickness is 1.5 nm for both top and bottom gates, and the silicon film thickness is 3.6 nm. The transverse effective mass $m_t = 0.19$ m_o (mass in x-y pane i.e. m_{x-y}) and $m_l = 0.91$ m_o (mass in z pane i.e. m_z), threshold voltage, $V_T = E_F/q = 0.2$ V. Fig. 2(b) shows

the variation of calculated drain current (I_D) as a function of drain voltage at a different gate voltage (i.e. at $V_G = 0.3$V and $V_G = 0.4$V) for common source characteristics at room temperature. Fig. 2(a) is the plot of computed $n_D(V_D)/n_D$ ($V_D = 0$) versus V_D. This revels that carrier density is approximately same as Drain Voltage varies. Let us consider the solution of equation first and fourth for two cases: - First, assume C_{OX} is small, than a small change in n_s has a large effect on $E_i(0)$, according to first equation. Now on increasing drain voltage, n_s will decreases according to (4).But according to equation (1) n_s will, in turn, decrease $E_i(0)$. But again equation (4) revels that smaller $E_l(o)$ will increase n_s.Hence this feedback mechanism keeps n_s fixed with drain bias. For large C_{OX} equation (1) shows that $E_l(0)$ will be set directly by the gate voltage. From above discussion, we consider that for small C_{OX}, the gate voltage controls the potential of the top of the barrier.

5. CONCLUSIONS

In this study, the electrostatics of nano transistor has been investigated by considering the 2-D electrostatics and quantum capacitance. We conclude that the Si/SiO$_2$ interface, that trap mobile charge carriers and cause a potential or even a full depletion of MOS Transistor, strongly influence the electrical properties of nano transistor. Simple formulas to estimate the self-Consistent Potential, Quantum capacitance hence current have been presented.

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