J. Nano- Electron. Phys.
3 (2011) No1, P. 569-575

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PACS numbers: 85.30.Tv, 85.35. – p

TWO DIMENSIONAL ANALYTICAL MODELING FOR SOI AND SON MOSFET AND THEIR PERFORMANCE COMPARISON

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During last few decade continuous device performance improvements have been achieved through a combination of device scaling, new device structures and material property improvement to its fundamental limits. Conventional silicon (bulk CMOS) technology can't overcome the fundamental physical limitations belong to sub-micro or nanometer region which leads to alternative device technology like Silicon-on-Insulator (SOI) technology and its recent innovative modification Silicon-On-Nothing (SON) MOSFET. Analytical simulation is very important to understand the relative performance of those devices under different structural and operational parameter variations. For present analytical simulation asymmetric structure of Silicon-On-Insulator (SOI) MOSFET and Silicon-On-Nothing (SON) MOSFET are considered. The proposed structure of SON MOSFET is similar to that of the SOI MOSFET with the only exception being the oxide layer here is substituted with air which has much lower permittivity than Silicon-dioxide. Variation of threshold voltage against effective channel lengths is compared for both the structures. From our simulation it is observed that the proposed SON model has lower drain to source current (I_{DS}) than SOI model. In our modeling based on solution of two dimensional Poisson's equation short channel effects such as DIBL and fringing field effects are also taken into account. SON is found to provide better suppression of SCE s than SOI. The results predicted by our analytical simulation hold good agreement with experimental results.

Keywords: *THRESHOLD VOLTAGE, SOI/SON MOSFET, SHORT CHANNEL EFFECTS, JUNCTION CAPACITANCE, POTENTIAL PROFILE, DIBL, FRINGING FIELD EFFECTS.*

(Received 04 February 2011)

1. INTRODUCTION

Fully-depleted CMOS/SOI devices offer superior electrical characteristics over bulk CMOS devices [1] such as reduced junction capacitances, increased channel mobility, suppressed short-channel effect, excellent latch up immunity and improved sub threshold characteristics [2]. SOI MOSFET has all the same features of a bulk MOSFET except there being an oxide layer between the channel and the substrate. The oxide layer is known as buried oxide layer. This has much greater Short Channel Effect suppressing capability than normal Silicon MOSFET structure. In a fully-depleted SOI structure the electrostatic coupling of channel with source/drain and

substrate through the buried layer (BL) [3] is reduced. Reduced coupling effect initiates less SCE s and thus allows further device scaling [4]. Evidently SOI is the better of the two candidates for device miniaturization. It can be scaled to low dimension with the performance not being affected much by SCE. Nowadays a newer proposed model is being considered, namely Silicon-on-Nothing. Here the oxide layer is comprised of air instead of Silicon-dioxide. As air is the highest insulating material only next to vacuum hence SON has better SCE immunity even than SOI. The proposed SON structure exhibits lower drain current and better threshold voltage roll-off for given physical parameters. Our analytical model using Poisson's equation has been presented for the surface potential leading to the threshold voltage model for the SOI/SON MOSFET. The accuracy of the model is verified by comparing with the experimental results as given by [5].

2. THE ANALYTICAL MODEL

In a short channel device, potential profiles in the channel and beneath the channel (in the BL) are two-dimensional [6]. Threshold voltage of the device can be calculated by solving 2-D Poisson's equation in the channel [7]. A general layered structure of a SOI MOSFET with polysilicon (n^+) as gate is shown in Fig. 1. We take t_f, t_{Si}, t_b and t_{sub} to be the thicknesses of gate oxide, silicon channel layer, buried layer and the substrate layer, respectively.

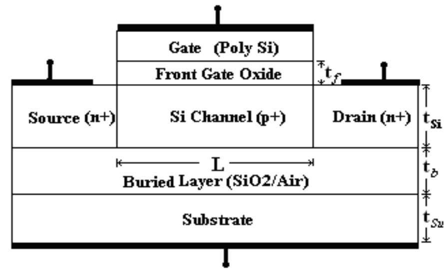

***Fig. 1** – A general SOI/SON-MOSFET layered structure*

Also let L be the metallurgical channel length of the device. The 2-D Poisson's equation applied to the two dimensional channel region of the depleted silicon film body ($0 \le x \le L$, $0 \le y \le t_{Si}$) is as in [6],

$$\frac{\partial^2\Psi(x,y)}{\partial x^2} + \frac{\partial^2\Psi(x,y)}{\partial y^2} = \frac{qN_A}{\epsilon_{Si}} \quad (1)$$

where, $\Psi(x, y)$ is the 2-D potential profile in the silicon channel, N_A is the doping concentration of the p-type substrate and ϵ_{Si} is the permittivity of silicon.

We consider a second order potential approximation for $\Psi(x, y)$ as per Young [8];

$$\Psi(x, y) = A_1(x) + A_2(x)y + A_3(x)y^2 \quad (2)$$

Now let the surface electrostatic potential at the front gate oxide/silicon film interface be $\Psi_{sf}(x)$ and that at the back buried oxide/silicon film interface as $\Psi_{sb}(x)$. The four boundary conditions in the channel at the channel-front gate oxide interface and channel-buried oxide interface, source side and drain side are given as [7];

At $y = 0$,

$$\frac{\partial\Psi(x,y)}{\partial y} = -E_{sf}(x) = -\frac{\in_{Ox}}{\in_{Si}}\frac{\left[V'_{gs} - \Psi_{sf}(x)\right]}{t_{Ox1}} \tag{3}$$

At $y = t_{\mathrm{Si}}$,

$$\frac{\partial\Psi(x,y)}{\partial y} = -E_{sb}(x) = -\frac{\in_{Ox}}{\in_{Si}}\frac{\left[V'_{ss} - \Psi_{sb}(x)\right]}{t_{Ox2}} \tag{4}$$

At $x = 0$,

$$\Psi(0,0) = \Psi_{sf}(x)\big|_{x=0} = V_{bi} \tag{5}$$

At $x = L$,

$$\Psi(L,0) = \Psi_{sf}(x)\big|_{x=L} = V_{bi} + V_{DS} \tag{6}$$

where $\in_{\mathrm{Si}}$ and $\in_{\mathrm{Ox}}$ are dielectric permittivity of silicon and oxide, respectively. V'_{gs} and V'_{ss} are the effective front gate to source and substrate to source voltages.

$$V'_{gs} = V_{gs} - V_{ffb},\ V'_{ss} = V_{ss} - V_{bfb}$$

V_{ffb} and V_{bfb} being the front and back gate flatband voltages respectively. Solving Eqn. (1) and (2) with the first two boundary conditions (Eqn. 3 & 4) we get the threshold voltage as [6, 7, 9];

$$V_{th} = V_{ffb} + \frac{\left[1 + \frac{c_f}{c_b} + \frac{c_f}{C_{Si}}\right](2\varnothing_F)}{\left[\frac{c_f}{c_b} + \frac{c_f}{C_{Si}}\right]} + \frac{qN_A t_{Si}\left[1 + 2\frac{c_{Si}}{c_b}\right]}{2c_{Si}\left[\frac{c_f}{c_b} + \frac{c_f}{C_{Si}}\right]} - \frac{V'_{ss}}{\left[\frac{c_f}{c_b} + \frac{c_f}{C_{Si}}\right]} \tag{7}$$

where, V_{th} represents the long channel threshold voltage and $2\varnothing_F = kT/q\ln(N_A/n_i)$ is the Fermi potential in the silicon film. Now V_{ss} is modified into V_{sseff} as,

$$V_{sseff} = V_{ss} + \frac{t_{Ox2}^2}{L^2}\left[kV_{ds} + rE_0 L\right] \tag{8}$$

By substituting the value of the lateral field E_0 in Eqn. 8, we find V_{sseff} as,

$$V_{sseff} = V_{ss} + \frac{t_{Ox2}^2}{L^2}\left[kV_{ds} + r\left(-\frac{2c_{Si}+c_f}{2c_{Si}+c_b}\frac{(V_{bi}+V_{ds}-V')-(V_{bi}-V')\cosh\left(\frac{L}{\lambda}\right)}{\lambda\sinh\left(\frac{L}{\lambda}\right)}\right)L\right] \quad (9)$$

Putting V_{sseff} in the Eqn.7 we will get the expression of modified threshold voltage as;

$$V_{theff} = V_{ffb} + \frac{\left[1+\frac{c_f}{c_b}+\frac{c_f}{C_{Si}}\right](2\varnothing_F)}{\left[\frac{c_f}{c_b}+\frac{c_f}{C_{Si}}\right]} + \frac{qN_A t_{Si}\left[1+2\frac{c_{Si}}{c_b}\right]}{2c_{Si}\left[\frac{c_f}{c_b}+\frac{c_f}{C_{Si}}\right]} - \frac{V_{sseff}^{'}}{\left[\frac{c_f}{c_b}+\frac{c_f}{C_{Si}}\right]} \quad (10)$$

Now using last two boundary conditions (Eqn. 5 & 6) we get the actual short channel threshold voltage as;

$$V_{thsc} = V_{theff} + \frac{1}{K_3}\left[\frac{2\varnothing_F}{K_1} - \frac{K_1}{K_2} - \varnothing_F\right] \quad (11)$$

Where,

$$K_1 = \frac{V_{bi}\left[\sinh\left(\frac{L-x_{\min}}{\lambda}\right)+\sinh\left(\frac{x_{\min}}{\lambda}\right)\right]+V_{ds}\sinh\left(\frac{x_{\min}}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}$$

$$K_2 = 1 - \frac{\left[\sinh\left(\frac{L-x_{\min}}{\lambda}\right)+\sinh\left(\frac{x_{\min}}{\lambda}\right)\right]}{\sinh\left(\frac{L}{\lambda}\right)}$$

$$K_3 = \frac{\left[\frac{c_f}{c_b}+\frac{c_f}{C_{Si}}\right]}{\left[1+\frac{c_f}{c_b}+\frac{c_f}{C_{Si}}\right]}$$

The drain current is formulated from threshold voltage as per [6] where

$$IDS = \frac{W\mu_{sff}U_f}{L\left(1+\frac{V_{DS}}{LE_c}\right)}\left[(V_{GS}-V_{th})V_{DS}-\frac{1}{2}V_{DS}^2\right] \quad (12)$$

in the linear region and

$$IDS = \frac{W\mu_{sff}U_f}{L\left(1+\frac{V_{DSsat}}{LE_c}\right)}\left[(V_{GS}-V_{th})V_{DSsat}-\frac{1}{2}V_{DSsat}^2\right] \tag{13}$$

in the saturation region.

where E_C is the critical field at which electron velocity (υ_e) saturates and $V_{DS,sat}$ is the saturation voltage and both are given by,

$$E_c = \frac{\upsilon_s}{\mu},\ V_{DSsat} = \frac{V_{GS}-V_{th}}{1+\frac{V_{GS}-V_{th}}{LE_c}}$$

3. RESULTS AND DISCUSSION

In bulk MOSFET only front interface surface potential ϕ_{sf} is affects the threshold voltage whereas in short channel SOI structure, ϕ_{sf} as well as back interface ϕ_{sb} strongly influences the threshold voltage. Here performance of SOI structure is simulated with respect to the threshold voltage which can be explained on the basis of relative coupling of front and back interface potential. Significant modification of ϕ_{sb} in SON structure due to lowest dielectric constant material (air) in the box region will initiate signification performance variation over SOI structure. Whole set of results presented here, regarding the threshold voltage and drain current can be explained on the basis of relative variation of front and back interface potential. Value of potential coupling ratio ($P_{CR} = \phi_{sf}/\phi_{sb}$) gives an estimation of SCEs and on the basis that performance of SOI and SON structures are compared. Higher P_{CR} initiates less SCEs specially DIBL which can be initiated with higher ϕ_{sf} or lessϕ_{sb}.

Increasing channel length shifts the short channel device towards bulk. With increasing channel length the value of the minimum surface potential reduces further therefore increasing the threshold voltage. SON suffers lesser potential coupling than SOI due to the fact air having much higher permittivity than Silicon-dioxide. Evidently SON has higher threshold voltage than SOI. From Fig. 2. it is quite clear that SON structure shows improvement in Threshold Voltage Roll-Off (*TVRO)* compared to SOI structure.

Now among the two devices, as the threshold voltage of the SON is more hence for the same applied gate voltage lesser number of inversion charge carriers are generated in the channel region of SON. Evidently SON has lower drain current than SOI as seen in Fig 3.Also as gate voltage increases carrier generation increases which results in more drain current for both the devices. Drain currents from analytical models of SOI and SON are compared with experimental results. Excellent agreement between the analytical model and experimental results [5] substantiates the validity of our model.

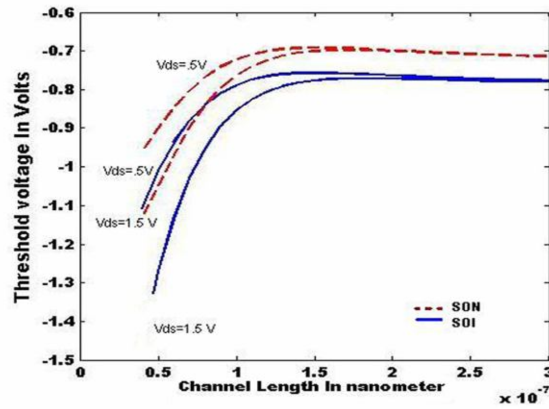

Fig. 2 – *Threshold Voltage variation against diff. channel lengths for applied* V_{DS} = 5 *Volts and* 1,5 *Volts*

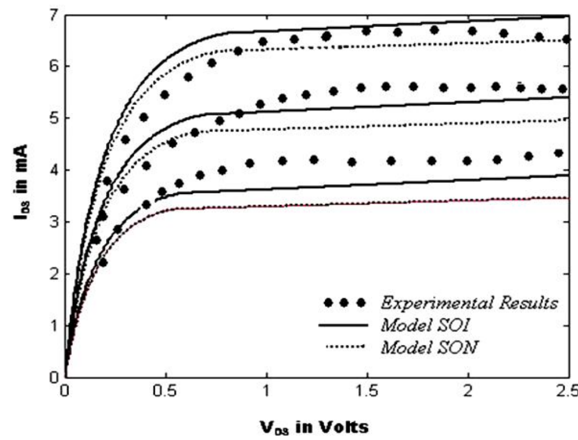

Fig. 3 – *Variation of drain current against drain to source voltages for gate to source voltages of* 2 *Volts,* 2,5 *Volts and* 3 *Volts*

4. CONCLUSION

A generalized threshold voltage model for SOI/SON-MOSFET is developed by solving 2-D Poisson's equation in the channel region and analytical expressions are also developed for the same. The performance of the devices is studied with respect to threshold voltage and drain current. Of the two devices for the same dimension and parameters SON has more threshold voltage and lower drain current. But to reduce P_{CR} further material with higher dielectric constant material at the gate oxide layer can be used. Present analytical SON device model can be used in the next generation SON based circuit simulator due to its simplicity and faster convergence property.

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